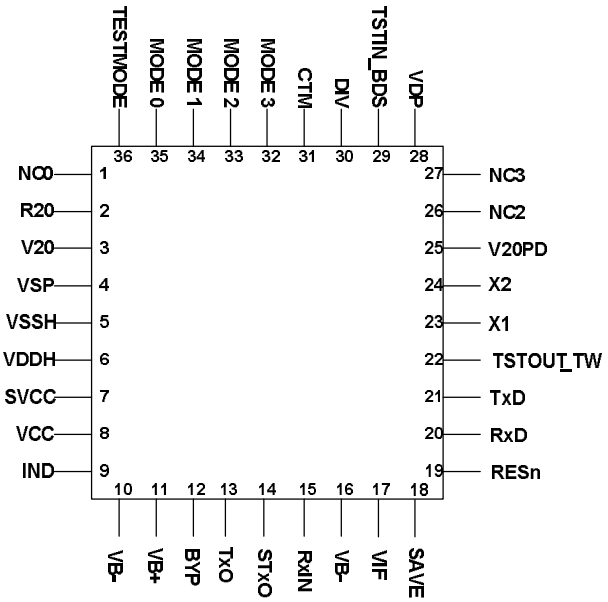
KNX EIB TP-UART 2+ - IC



Features

- Signaling for standard UART (LSB-First, Idle is 1)
- Baud rate 115200 or 19200 for the communication: TP-UART 2+ ←→ Host – Controller
- Direct coupling to host controller (TxD, RxD), or via optical couplers (optional)
- 2-wire protocol with software handshake
- Buffering of sent frames
- No critical timing during transmission
- VCC switchable between 3.3 V and 5 V
- Efficiency of VCC-supply ≥ 75 %
- $I_{VCC} \leq 30mA$ (50 mA if no load at V20)
- Switchable V20 power supply 20V/25mA with limiting function
- I_{V20max} adjustable in steps
- IVB+max overshoot due to load changes actively limited
- Operating temperature range: -25°C to 85°C
- Small QFN36X36 package

GENERAL DESCRIPTION

The TP - UART - IC (**T**wisted **P**air - **U**niversal **A**synchronous **R**eceive **T**ransmit - IC) is a transceiver which supports the connection of microcontrollers of sensors, actuators, or other applications to the EIB (**E**uropean - **I**nstallation - **B**us).

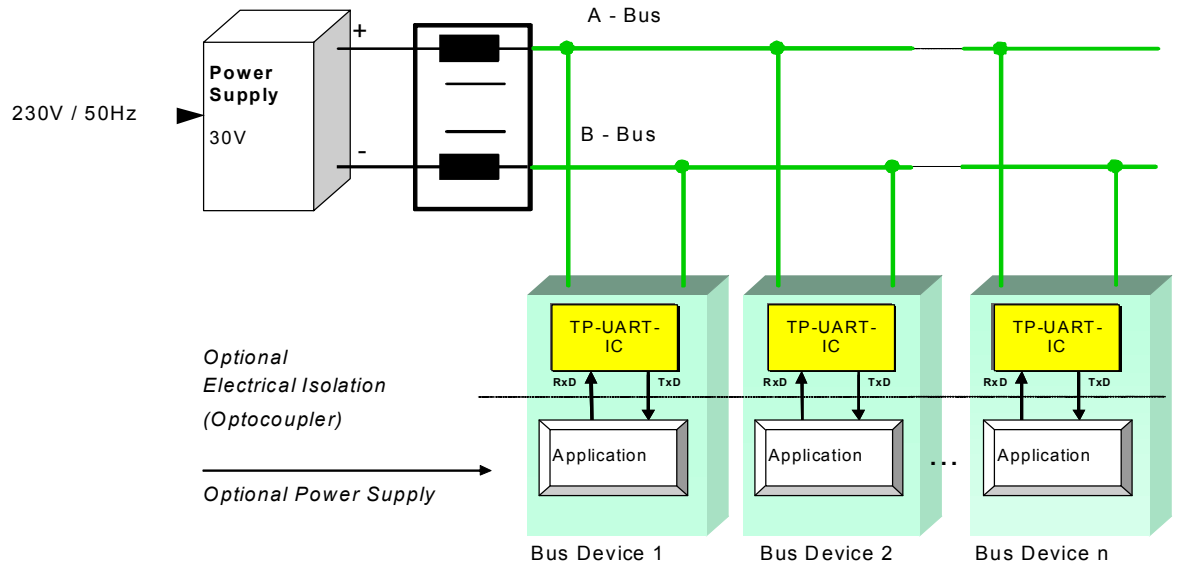
This module supports every transmit- and receive - function and also the high ohmic decoupling of energy from bus line. It generates further a stabilized 3.3V or 5V supply to use by a host controller. Up to 256 subscribers can be connected to one bus line.

An UART interface is realized for communication with a host controller. The coupling can be realized directly or via optical couplers.

The TP - UART - IC consists of two main parts: the digital part (UART - Interface) and the analog part (analog circuit part).

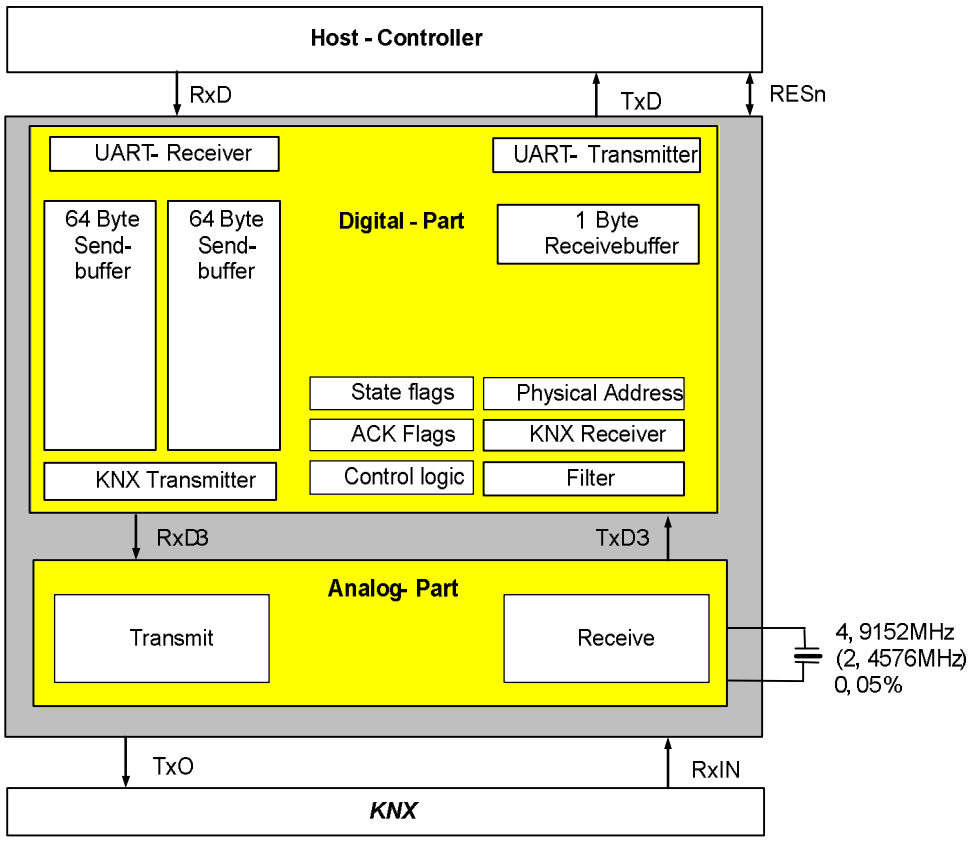
KNX EIB TP-UART 2+ - IC

GENERAL DRAWING



STRUCTURE OF TP-UART 2+ - IC

(Block Diagram)



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KNX EIB TP-UART 2+ - IC

TABLE OF CONTENTS

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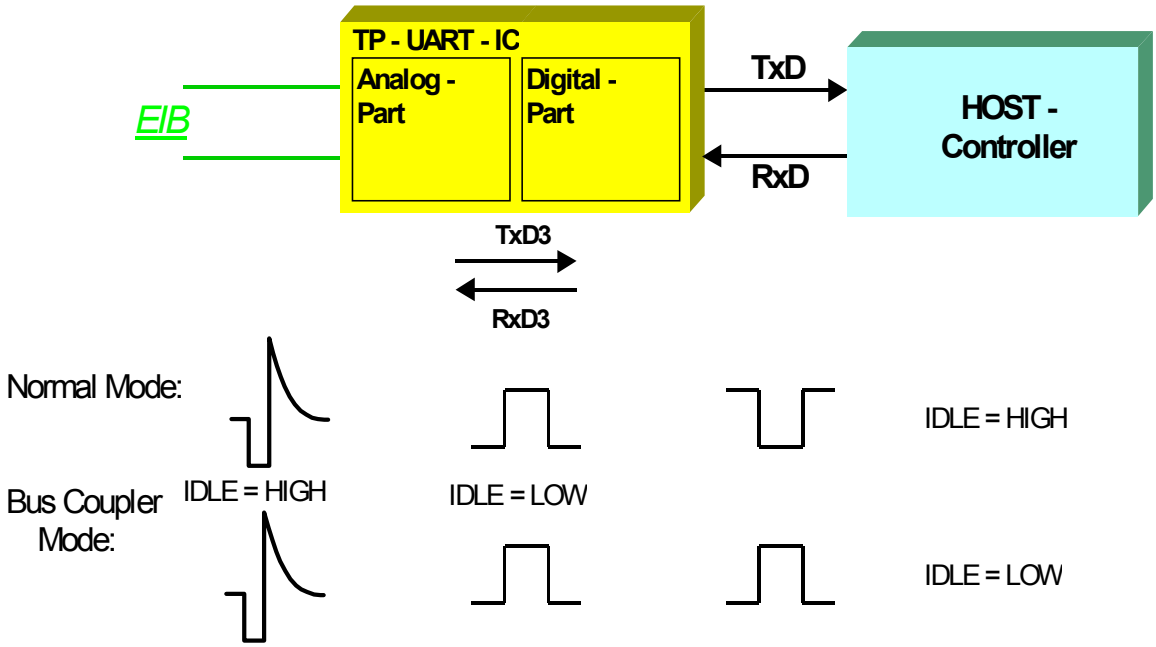
KNX EIB TP-UART 2+ - IC

1 Modes of Operation

1.1 Interface to host electronics



1.2 Selection of Different Modes of Operation

Mode of operation	MODE				TEST MODE	CTM	TSTIN_BDS	TSTOUT_TW
	0	1	2	3				
Normal	1	1	0	0	0	0	BDS=0: 19.2 kBd at UART BDS=1: 115.2 KBd at UART	TW
Analog	1	0	0	0	0	0	0	TW

Table 1: Modes of Operation

2 The ANALOG – PART

2.1 Package and Pin Definitions

2.1.1 Package Pin Assignment

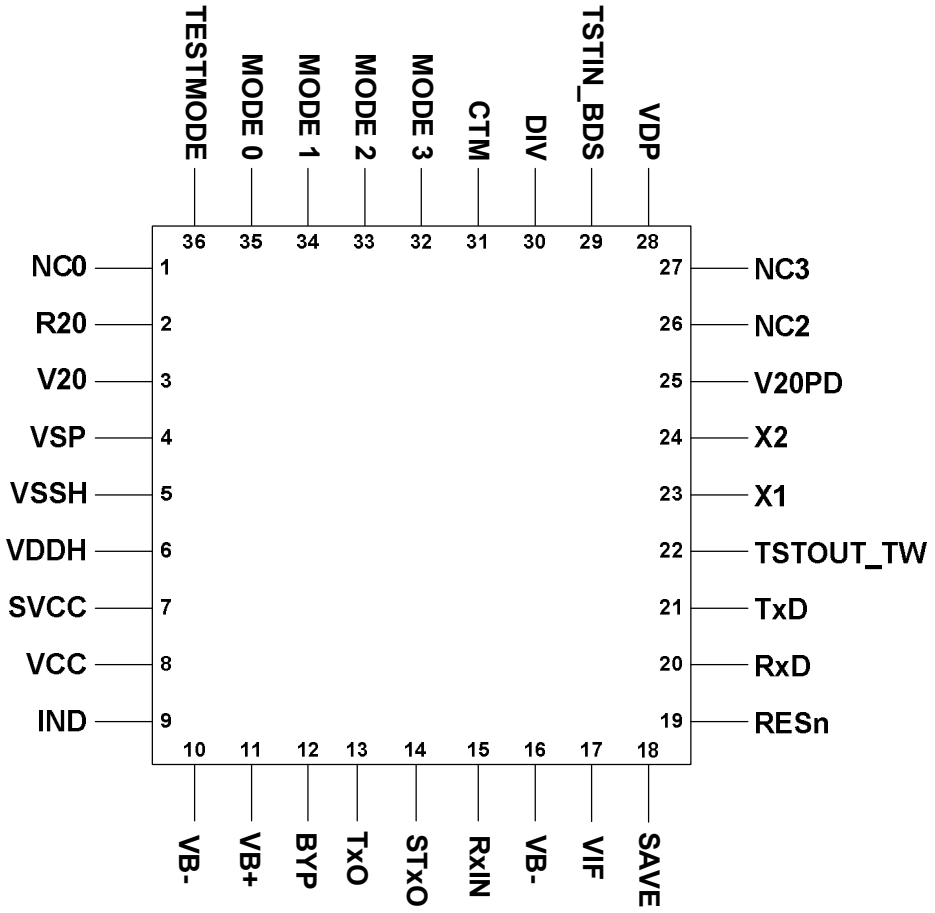


Figure 1 Package Pin Assignment

2.1.2 PIN DESCRIPTION

Pin	Pin Name	Pin Type	Positive supply	Negative supply	Notes
1	NC0	AIO	VB+	VB-	Used during chip test mode
2	R20	AIO	VDP	VB-	External resistor to VB- sets V20 max current
3	V20	AIO	50V Clamp to VB-	VB-	Internally generated 20V power supply
4	VSP	AIO	50V Clamp to VB-	VB-	Intermediate voltage blocking capacitor
5	VSSH	AIO	VSP	VB-	SMPS control

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6	VDDH	AIO	VSP	VB-	SMPS control
7	SVCC	AIO	VCC	VB-	VCC control
8	VCC	AIO	5.5V Clamp to VB-	VB-	External power supply 3.3/5 V
9	IND	AIO	VSP	VB-	SMPS-output; no external freewheeling diode
10	VB-	S	Ground		Negative bus pin, exposed pad (see Figure 5 and 7.2 Layout Guidelines)
11	VB+	S	70V Clamp to VB-	VB-	Positive bus pin
12	BYP	AIO	VB+	VB-	Bypass current stabilisation pin
13	TXO	AIO	VB+	VB-	Transmit output current (bus signal)
14	STxO	AIO	VB+	VB-	Transmitting active indication
15	RxIN	AIO	VB+	VB-	Capacitive coupled to bus signal
16	VB-	S	Ground	Negative bus pin	
17	VIF	S	5.5V Clamp to VB-	VB-	External supply for IO cells
18	SAVE	DO_PU	VIF	VB-	Signalization of bus voltage break-down
19	RESn	DIO_PU	VIF	VB-	Reset pin, open drain with internal pullup
20	RxD	DI_PD	VIF	VB-	Data receive from host with internal pulldown
21	TxD	DO	VIF	VB-	Data transmission to host
22	TSTOUT_TW	DO	VIF	VB-	Digital test / temperature signal
23	X1	DI	VIF	VB-	Crystal oscillator pin 1; external clock input
24	X2	DO	VIF	VB-	Crystal oscillator pin 2
25	V20PD	DI	VDP	VB-	Enable and disable V20
26	NC2	DIO	VDP	VB-	Used during chip test mode
27	NC3	AIO	VDP	NA	
28	VDP	AIO	5.5V Clamp to VB-	VB-	Storage capacitor for internal power supply
29	TSTIN_BDS	DIO	VDP	VB-	Input for digital test / baud rate select; digital output for analog test
30	DIV	DI	VDP	VB-	Internal clock divider 2:1 active
31	CTM_AMS	DI	VDP	VB-	Chip Test mode control
32	MODE 3	DI	VDP	VB-	Chip Test Mode control pin 4
33	MODE 2	DI	VDP	VB-	Chip Test Mode / Mode control pin 3
34	MODE 1	DI	VDP	VB-	Mode control pin 2
35	MODE 0	DI	VDP	VB-	Mode control pin 1
36	TESTMODE	DI	VDP	VB-	Test mode control

Table 2: Pin Description

PIN Types:
- S ... supply pad
- AIO ... analog I/O
- DI … digital input
- DI_PU ... digital input with pull-up

DI_PD ... digital input with pull-down
DIO_PU ... digital I/O with pull-up
DO ... digital output
DO_PU ... digital output with pull-up
NC ... Not connected. Recommend to be tied to VB- in the application.

2.2 OPERATING CONDITIONS

2.2.1 General operating conditions

All specification parameters, unless otherwise stated, are valid within the General operating conditions. Unless otherwise stated all voltages are referenced to the VB- pin.

Symbol	Parameter	Min	Max	Unit	Note
VB+	positive line voltage	11	45	V	1)
V_{CC}	positive supply voltage for external supply	5.0 - 5%	5.0 + 5%	V	2)
	(digital test modes with SHB = 0)	3.3 - 5%	3.3 + 5%	V	2)
V_{IF}	positive external supply voltage	3.0	5.5	V	
T_{amb}	ambient temperature	-25	85	ºC	
T_{jnc1}	Junction temperature		125	ºC	
f_{clk}	clock frequency (external quartz)		4.9152	MHz	3)

1) DC voltage of bus is 20V to 30V, with signal and compensation pulse 11 V ... 45 V
2) set by SVCC
3) 4.915MHz external clock running

Table 3 General operating conditions

2.2.2 ABSOLUTE MAXIMUM RATINGS (NON OPERATING)

Stresses beyond those listed under “Absolute Maximum Ratings“ may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under “Operating Conditions” is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Unless otherwise stated all voltages are referenced to the VB- pin.

Parameter	Symbol	Min	Max	Unit	Note
positive line voltage	VB+	-0.3	50	V	1)
positive supply voltage (internal or external supply)	V_{CC}	-0.3	7	V	2)
positive external supply voltage	V_{IF}	-0.3	7	V	2)
intermediate voltage (generated by on-chip regulator)	V_{VSP}	-0.3	50	V	2)
voltage on pin TxO	V_{TxO}	-0.3	50	V	1)
voltage on pin RxIN	V_{RxIN}	-0.3	50	V	1), 4)
voltage on pin BYP	V_{BYP}	-0.3	50	V	1)
voltage on pin STxO	V_{STxO}	-0.3	50	V	1)

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Parameter	Symbol	Min	Max	Unit	Note
voltage on pin V20	V_{20}	-0.3	25	V	2)
voltage on pin IND	V_{IND}	-0.3	50	V	
voltage on low voltage pins MODE0, MODE1, MODE2, MODE3, TSTIN_BDS, TESTMODE, DIV, SVCC, CTM	V_{LV1}	-0.3	V_{DP} +0.5	V	9)
voltage on low voltage pins TxD, RESn, TSTOUT_TW, X1, X2, RxD, SAVE	V_{LV2}	-0.3	V_{IF} +0.5	V	5)
Internal supply voltage to digital part	V_{VDP}	-0.3	5	V	
voltage used for internal DC/DC-converter	V_{VDDH}	-0.3	50	V	
voltage used for internal DC/DC-converter	V_{VSSH}	-0.3	50	V	
Ambient temperature	T_{amb}	-25	85	^{o}C	
Junction temperature	T_j		145	^{o}C	
storage temperature	T_S	-65	150	^{o}C	
ESD stress voltage that will not cause damage to the device	V_{ESD}		± 1200	V	3)
static current for latchup initialization	$I_{LATCHUP}$	± 50		mA	
thermal resistance of QFN package to ambient	R_{tha}		28	K/W	6)
thermal resistance of QFN package to package surface measured on exposed paddle	R_{ths}		5	K/W	6)
Total power dissipation at T_{amb} = 85^{o} C (all supplies and outputs)	P_t		1.4	W	TW not active 7)
Humidity non-condensing	H_{NC}	5	93	%	8)

Table 4 Absolute maximum ratings

Notes:

(1) during surge impulse: -20 V for 2 µsec and +65 V for 150 µsec

(2) In particular allowed voltage relations (no damage under following voltage relations):
- (a) $V_{VSP} \geq$ VB+; e.g. VB+ = 0 V due to a short circuit
- (b) $V_{V20} \geq V_{VSP;}$ e.g. V_{VSP} = 0 V due to a short circuit or VB+ = 0 V
- (c) $V_{VCC} \geq V_{VSP;}$ e.g. V_{VSP} = 0 V due to a short circuit or VB+ = 0 V
- (d) $V_{IF} \geq V_{VCC}$; e.g. when an external supply for V_{IF} is used and VB+ = 0 V
- (e) V_{CC} and V_{VSP} normal / VB+ and V_{IF} can be 0 V
- (f) V_{VSP} normal / V_{CC} , VB+ and V_{IF} can be 0 V
- (g) V_{IF} normal / V_{CC} , VB+ and V_{VSP} can be 0 V
- (h) $V_{DP} \geq V_{VSP}$; e.g during normal startup sequence.

(3) human body model: 100 pF, 1.5 kΩ, Mil. Std. 883, method 3015.7

(4) dynamic via C_{REC}= 47 nF in case of switching-on/off the bus voltage, complies with V_{CREC} at normal operation, may be down to -20 V.

(5) max. 7 V
(6) Measurement conditions in accordance with EIA/JEDEC STANDARD 51-2. Value is an estimate only.
(7) For $R_{th} \leq 28k/W$
(8) Valid susceptibility against humidity is described by JEDEC JESD22-A112, table 1, level 5
(9) Max. 5V

2.2.3 Quality Issue

60 FIT at 70 °C

2.2.4 Bus Pins VB+ and VB-

Via these pins the ASIC is connected to the bus lines. External diode to prevent reverse bias of ASIC and external suppressor diode to limit the burst pulses are required.

Symbol	Parameter	Min	Max	Unit	Note
V_{VB+}	positive line voltage	-0.3	45	V	1)
I_{analog}	current consumption in analog mode (without external clock)		1	mA	2) 4)
I_{normal}	current consumption in normal mode (with external clock)		2.1	mA	3) 4)
I_{analog}	current consumption in analog mode (without external clock)		1	mA	2) 5)
I_{normal}	current consumption in normal mode (with external clock)		2.1	mA	3) 5)

1) DC voltage of bus is 20V to 30V. During surge impulse: -20 V for 2 µs and 65 V for 150 µs
2) no load at all (VCC, V20, I/O-pins)
3) 4.915MHz external clock running
4) SVCC connected to VCC (nominal VCC = 5V)
5) SVCC connected to VB- (nominal VCC = 3.3V)

Table 5 Bus Pins VB+ and VB-

2.2.5 CCS stabilisation Pin BYP

The BYP pin drives the control node of the controlled current source (CCS) via a capacitor connected to the VB+ bus line. This drive is used to ensure that the capacitive loading on the EIB, by the ASIC, is below a specific value.

Symbol	Parameter	Min	Max	Unit	Note
V_{BYP}	Bypass voltage range	-0.3	45	V	1)
C_{BYP}	external coupling capacitance	44.5	49.5	nF	typ. 47 nF

1) DC voltage of bus is 20V to 30V. During surge impulse: -20 V for 2 µs and 65 V for 150 µs

Table 6 CCS stabilisation pin BYP

2.2.6 Buffer Voltage Pin VSP

The ASIC delivers a supply voltage of 3.3 or 5 volts to external loads. In order to prevent a rapid change of bus current in the case of a rapid change of external load an external capacitor at the pin VSP is used for energy storage. The static voltage at VSP is adjusted to V_{VB+} - V_{VDIF}. V_{VSP} is connected by a short circuit to pin VDDH externally in the application. VDDH is used as the input for the VCC DC-DC converter and the VSSH regulator. VSP is used as the input for V20 linear regulator and VDP linear regulator.

Symbol	Parameter	Min	Max	Unit	Note
V_{VSP}	energy buffer voltage	V_{VB+} - V_{VDIF}	30	V	1)
V_{VDIF}	voltage difference between V_{VB+} and V_{VSP}	0.5	2	V	
C_{VSP}	external storage capacitance	120		µF	2) 6)7)
ESR_{VSP1}	ESR of external storage capacitance evaluated @ 120Hz		0.70	Ω	8)
ESR_{VSP2}	ESR of external storage capacitance evaluated @ 100kz		0.20	Ω	8)

1) DC voltage of bus is 20V to 30V.
2) recommended 330 µF; must be larger than the capacitor at VCC
6) It is highly recommended, but not mandatory, that an additional capacitor C_{VDDH} is included in any application configuration where capacitors C_{VSP} is present. When present it is recommended that C_{VDDH} be placed as close as possible to pin VDDH.
7) C_{VSP} affects the max. allowed load current at VCC and V20 (see 2.2.7 and 2.2.10).
If $C_{VSP} < 330$ µF ±20% fan in has to be multiplied by 264µF/C_{VSP}.
There are no restrictions if $C_{VSP} \geq 264$ µF (Therefore 330 µF ± 20 % is recommended.).
8) If $C_{VSP} < 330$ µF ±20% ESR has to be multiplied by 264µF/C_{VSP}.

Table 7 Buffer Voltage Pin VSP

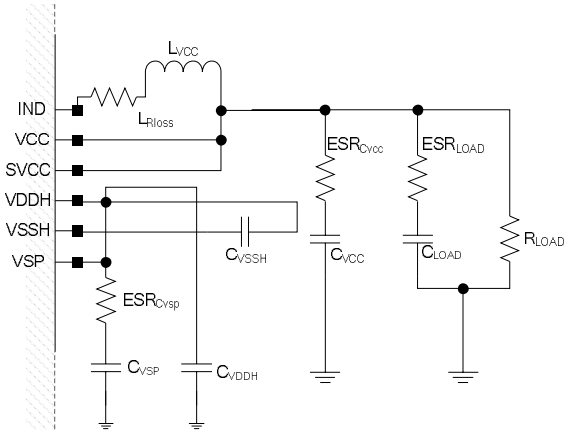

Figure 2 VCC supply external connections

2.2.7 Supply Pin VCC

Pin VCC delivers the internally generated supply voltage to external loads. The supply is generated by a switched mode power supply (with an internal oscillator, softstart function), current source and shunt regulator. The voltage of VCC depends on the level of pin SVCC. Internal input voltage for VCC (switched mode power supply) is VDDH. VCC supply generation is disabled during softstart.

The I_{VCC} maximum current can be greater than 30mA if the maximum I_{V20} current is reduced.

Symbol	Parameter	Min	Max	Unit	Note
V_{IN}	input voltage	6.25	33	V	
$V_{VCC[5]}$	supply voltage (generated by the ASIC)	5.0-5%	5.0+5%	V	1)
$V_{VCC[3]}$	supply voltage (generated by the ASIC)	3.3-5%	3.3+5%	V	2)
C_{VCC}	external storage capacitance	8	18	µF	
L_{VCC}	External Inductance	220		µH	
L_{VCC}	External Inductor	Series loss resistance ≤ 7.5Ω			3)4)
C_{VCCESR}	ESR of external storage **and** load capacitance to achieve $V_{ripple1}$	0.3	0.7	Ω	
I_{VCC}	external load at VCC	0	30	mA	5)
	with reduced I_{V20}		50	mA	5)

1) SVCC connected to VCC
2) SVCC connected to VB-
3) Such as EPCOS SIMID B824432C part No. B824321224K000
4) If series loss resistance ≤ 1 Ω an efficiency of typical 80 % will be reached
5) If C_{VSP} < 330 µF ±20% the current value has to be divided by 264µF/C_{VSP} (see Table 7).

Table 8 Supply Pin VCC

2.2.8 Supply Pin VDP

Pin VDP delivers an internally generated supply voltage to internal loads only. The supply is generated by a series regulator. Internal input voltage for VDP is VDDH. Supply VDP is the positive supply for the mode control pins and DIV and TSTIN_BDS pins.

Symbol	Parameter	Min	Max	Unit	Note
V_{IN}	input voltage	4.75	V_{VSP}	V	
V_{VDP}	Internal supply voltage	3.0	3.6	V	
C_{VDP}	external storage capacitance	176	264	nF	1)
I_{VDP}	external load at VDP		0	mA	2)

1) Low ESR < 0.1 Ohms
2) In the application there should be no external load on VDP.

Table 9 Supply Pin VDP

2.2.9 Supply Pins VDDH and VSSH

Pin VDDH and VSSH deliver an internally generated supply voltage to internal loads only. The VDDH supply is connected to the VSP externally by a short circuit. The VSSH supply is generated by a series regulator to provide a voltage to control the DC-DC converter. Internal input voltage for VSSH is VDDH which is supplied from the external voltage VSP.

Symbol	Parameter	Min	Max	Unit	Note
V_{VDDH}	Internal supply voltage	6.25	V_{VSP}	V	
V_{SSH}	Internal supply voltage	V_{VDDH}-3.6	V_{VDDH}-3.0	V	
C_{VSSH}	external storage capacitance	176	264	nF	1)
I_{VSSH}	external load at VSSH		0	mA	
I_{VDDH}	external load at VDDH		0	mA	

1) Low ESR < 0.1 Ohms

Table 10 Supply Pins VDDH & VSSH

2.2.10 Supply Pin V20 and Pin R20

Pin V20 delivers the internally generated supply voltage to external loads. The supply is generated by a series regulator. Internal input voltage for V20 is VDDH. The V20 regulator is switched off during softstart, making V20 unavailable

An external short-circuit from the V20 pin to VB- will not cause a destruction of the ASIC, interference on the bus or disturb generation of VCC. Relation V20(I_{V20}) shall have a fallback characteristic in order to limit the power loss.

The maximum current available from the V20 regulator can be reduced by adding an external resistance connected between the R20 pin and VB-. The R20 pin can be left open circuit if no reduction in maximum current is required.

In an applications where the V20 regulator is not going to be used pin 25 V20PD can be used to disable the V20 regulator. The pin should be hard wired to VB- for normal V20 operation and hard wired to VDP to disable the V20 regulator. The pin should not be used to dynamically control the state of the V20 regulator when the device is powered up. The CV20 capacitor can be removed from the application when V20PD is active (hard wired to VDP)

The IV characteristic of the regulated voltage should not cross the resistive load line defined by $R_{LL} = V_{V20(min)} / I_{V20}$.

Symbol	Parameter	Min	Max	Unit	Note
V_{V20}	supply voltage (when current limit is not active)	17.5	22.5	V	1)
C_{V20}	external storage capacitance	8	1200	µF	6)
C_{V20}	external storage capacitance when V20PD is active	0		µF	
I_{V20}	Load current with current limiting not active		25	mA	2)8)
I_{V20_ILIM}	Load current with current limiting active		30	mA	3)
I_{V20_SHORT}	Load current under short circuit conditions	5	16	mA	4)

1) $V_{VSP} \geq V_{V20} + V_{DROP}$; for static load currents in the range defined by I_{V20}; $V_{DROP} \leq 1V$
2) maximum allowed load at V20 for full output voltage.
3) current limitation of fallback characteristic
4) in case of short circuit: V20 connected with VB-, VB+=30V, VSP = 29.5V
5) power limitation of fallback characteristic
6) In parallel with ceramic 100nF
7) External resistor tolerance of ±1%
8) If $C_{VSP} < 330$ µF ±20% the current value has to be divided by 264µF/C_{VSP} (see´Table 7).

Table 11 Supply Pin V20

Symbol	Parameter	R20	Unit	IV20	Unit	Tol	Unit
R20	External maximum current setting resistance	262	kΩ	5	mA	0 to +5	mA
		345	kΩ	10	mA	0 to +5	mA
		520	kΩ	15	mA	0 to +5	mA
		1000	kΩ	20	mA	0 to +5	mA
		o/c	kΩ	25	mA	0 to +5	mA
Footnote 8) of Table 11 has to be considered.							

Table 12 External maximum current setting resistance

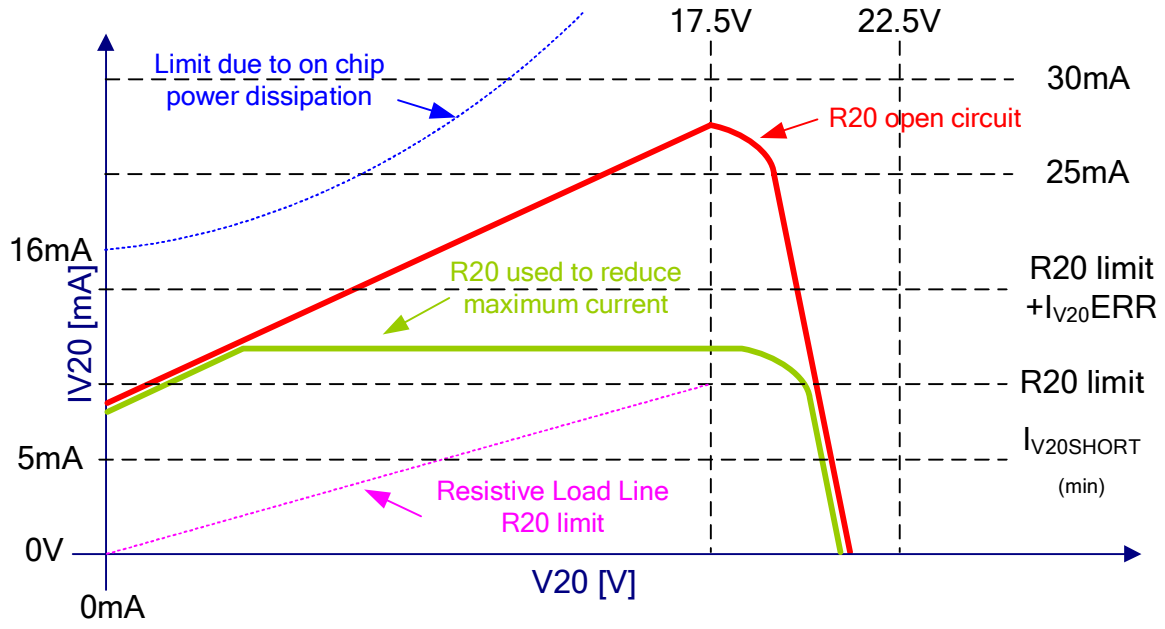

Figure 3 V20 Fallback Characteristic

2.2.11 Pin IND, SMPS-output

The pin IND is the output of the switched mode power supply. Internally the node is clamped to VB-. The voltages and currents depend on the switched mode power supply concept.

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2.2.12 Pin SVCC

This input pin controls the value of VCC. It is possible to switch between 3.3 V and 5 V. If pin SVCC is connected to VB-, VCC-voltage is 3.3 V. If pin SVCC is connected to VCC, VCC-voltage is 5 V. In any case it is necessary to connect SVCC to a defined level.

2.2.13 Receive Pin RxIN

The Receive Pin RxIN is coupled to the EIB bus by an external capacitor.

Symbol	Parameter	Min	Max	Unit	Note
C_{REC}	external coupling capacitance	44.5	49.5	nF	typ. 47 nF
1) AC coupled by external capacitor 47 nF± 5%					

Table 13 Receive Pin RxIN

2.2.14 Transmit Pin TxO

The transmit pin is connected to VB+ via external resistor of typ. 68 Ω.

Symbol	Parameter	Min	Max	Unit	Note
dV_{BUS}	delta(V_{BUS}) during active LOW pulse	-6	-9	V	1)
1) related to VB+					

Table 14 Transmit Pin TxO

2.2.15 Supply Pin VIF

The Pin VIF is used as supply voltage for the pins TxD, RxD, RESn, SAVE, TSTOUT_TW, X1, X2 and determines their high input or output level.

Symbol	Parameter	Min	Max	Unit	Note
V_{IF}	external supply voltage for interface	3.0	5.5	V	1)
C_{VIF}	external decoupling capacitor	10		nF	2)
1) typical supply voltages: 3.3 V or 5 V 2) recommended; should be placed as close as possible between VIF and adjacent VB- device pins.					

Table 15 Supply Pin VIF

2.2.16 Oscillator Pins X1 and X2

The oscillator Pins X1 and X2 are used for directly connecting a crystal of 4.9152 MHz without additional external capacitors. The tolerance of the oscillator is set by the parameters of the external crystal, and is expected to be +/- 0.05 %.

It is possible to drive the ASIC by an external clock by forcing the X1 with the external clock; pin X2 must be open

In Analog Mode no external XTAL is needed and the XTAL oscillator does not run. In this case X1 must be connected to VIF or VB-, X2 must be open.

Symbol	Parameter	Min	Max	Unit	Note
$V_{X1/2}$	Oscillator voltage at X1 and X2	-0.5	VIF + 0.5	V	
V_{IL}	voltage range for input low level		0.3 * VIF		
V_{IH}	voltage range for input high level	0.7 * VIF			
f_{clk}	clock frequency for external clock	2.4576	4.9152	MHz	1)2)
1) 4.9152 MHz or 2.4576 MHz, no other clock frequencies 2) Crystal Data (T_{amb}: -20 to 70 °C): 0 Ω ≤ E.S.R ≤ 91 Ω, C_L =16 pF (min: 15 pF, max. 21 pF), Drive $Level_{max.}$ = 60 µW, C_0 < 5 pF Crystal Data (T_{amb}: -25 to 85 °C): 0 Ω ≤ E.S.R ≤ 84 Ω, C_L =16 pF (min: 15 pF, max. 21 pF), Drive $Level_{max.}$ = 60 µW, C_0 < 5 pF					

Table 16 Oscillator Pins X1 and X2

2.2.17 Interface Pin RxD

The UART interface input pin RxD receives the information from host electronic to control the transmitter of the ASIC. This pin is an input pin with pull-down resistor. The switching levels are derived from external supply voltage VIF.
In normal mode: RxD = LOW → RxD3 = HIGH → transmitter switches on
In analog mode: RxD = HIGH → RxD3 = HIGH → transmitter switches on

Symbol	Parameter	Min	Max	Unit	Note
V_{IL}	voltage range for input low level		0.3 * VIF		
V_{IH}	voltage range for input high level	0.7 * VIF			
V_{hyst}	hysteresis for switching level	0.1 * VIF	0.4 * VIF		1)
$R_{PullDown}$	value of internal pull-down resistor	150	450	kΩ	
1) switching level approx. VIF/2, i.e. VIF/2 ± V_{hyst}/2					

Table 17 Interface Pin RxD

2.2.18 Interface Pin TxD

The UART interface output pin TxD transmits the information to host electronic. The high output level is derived from external supply voltage VIF.
In normal mode: LOW pulse at EIB bus → TxD3 = HIGH → TxD = LOW
In analog mode: LOW pulse at EIB bus → TxD3 = HIGH → TxD = HIGH

Symbol	Parameter	Min	Max	Unit	Note
V_{OH}	output voltage high	VIF - 0.5		V	I_{OH} = -5 mA
V_{OL}	output voltage low		0.4	V	I_{OL} = 5 mA
t_r, t_f	rise time, fall time (10 % ↔ 90 %)		100	ns	C_L = 150 pF

Table 18 Interface Pin TxD

2.2.19 Switching Pin STxO

The switching pin STxO is an open drain output with an external pull-up resistance. It is driven to provide a high output level during transmission. In all modes where the digital part is active an internal signal generated by the digital part and used to control the switching of STxO. It switches from LOW to HIGH before (typ. 500 µs) the first transmit signal. In all modes where the digital part is

not active Table 19 Switching Pin STxO applies. The control for the switching of STx0 is derived from the send pulse width limitation implemented within the analog part. The high output level is derived from an external supply voltage.

Symbol	Parameter	Min	Max	Unit	Note
V_{STx0}	External supply voltage for STx0	VIF	50	V	4)
V_{OH}	output voltage high		50	V	4) 5)
V_{OL}	output voltage low		0.4	V	I_{OL} = 5 mA
t_{DELAY}	delay time from active RxD to STxO L/H (50% $\leftrightarrow$ 50%)		300	ns	1) 2)
$t_{SENDMAX}$	delay time from inactive RxD to STxO H/L (50% $\leftrightarrow$ 50%)	1.5	2	ms	3)
t_r	rise time (10 % $\rightarrow$ 90 %)			ns	5)
t_f	fall time (90 % $\rightarrow$ 10 %) for V_{STx0}=30V		900	ns	C_L = 150 pF
	fall time (90 % $\rightarrow$ 10 %) for V_{STx0}=5.25V		100	ns	C_L = 150 pF

1) When the digital part is not active the STxO L/H is triggered / retriggered by an active RxD signal.
2) In normal mode the Digital part controls the STxO transitions with regard to the RxD signal.
3) When the digital part is not active.
4) during surge impulse: -20 V for 2 µsec and +65 V for 150 µsec
5) I_{OH} and t_r are set be external pull-up resistance.

Table 19 Switching Pin STxO

2.2.20 Reset Pin RESn

This pin is an I/O pin with internal pullup resistor to VIF. In reset case the reset pin delivers an active LOW signal to external host electronic. The output driver is realized as open drain. The reset state RESn = LOW can be caused by an internal or by an external RESET due to forcing an active LOW to the pin RESn. The switching levels are derived from external supply VIF.

Symbol	Parameter	Min	Max	Unit	Note
R_{PullUp}	value of internal pull-up resistor to VIF	10	25	kΩ	
V_{RESmax}	maximum voltage at RES pin		VIF + 0.5	V	
V_{IL}	voltage range for input low level	0	0.3 * VIF		
V_{IH}	voltage range for input high level	0.7 * VIF	1.0 * VIF		
V_{hyst}	hysteresis for switching level	0.1 * VIF	0.4 * VIF		1)
V_{OL}	output low voltage		0.2	V	2)
t_f	fall time (90 % $\rightarrow$ 10 %) for VIF = 5.25V		100	ns	C_L = 150 pF 3)

1) switching level approx. VIF/2, i.e. VIF/2 $\pm V_{hyst}/2$
2) I_{OL} of 1mA when VIF=1V; I_{OL} of 5mA when VIF ≥ 3V
3) Rise time determined by R_{PullUp}, C_L and VIF

Table 20 Reset Pin RESn

2.2.21 Mode Control Pins MODE0, MODE1, MODE2, MODE3 TESTMODE and CTM

These input pins are used to control the mode of the ASIC by connecting them to VB-(0) or VDP(1).

The normal operating mode is reached with MODE0 =1, MODE1 =1, MODE2=0, MODE3=0, TESTMODE =0 and CTM=0. Section 1.2 “Selection of Different Modes of Operation” shows the different modes selected by the MODE<0:2> and TESTMODE pins and the usage of the other pins in these modes.

Symbol	Parameter	Min	Max	Unit	Note
V_{IL}	voltage range for input low level	0	0.3 * VDP	V	
V_{IH}	voltage range for input high level	0.7 * VDP	1.0 * VDP	V	

Table 21 Mode Control Pins MODE0, MODE1, MODE2, MODE3, TESTMODE & CTM

2.2.22 Pin TSTIN_BDS

In normal mode it is used as input pin to select the baud rate of the UART interface to the host electronic.

Symbol	Parameter	Min	Max	Unit	Note
V_{IL}	input low level (UART baud rate 19.2 kBaud)	0	0.3 * VDP		
V_{IH}	input high level (UART baud rate 115.2 kBaud)	0.7 * VDP	1.0 * VDP		

Table 22 Pin TSTIN_BDS

2.2.23 Pin TSTOUT_TW

TW = HIGH means: chip temperature is higher than maximum allowed value and TxO is disabled.

Symbol	Parameter	Min	Max	Unit	Note
V_{OH}	Output HIGH voltage	VIF - 0.5		V	I_{OH} = -5 mA
V_{OL}	Output LOW voltage		0.4	V	I_{OL} = 5 mA
t_r, t_f	rise time, fall time (10 % ↔ 90 %)		100	ns	C_L = 150 pF

Table 23 Pin TSTOUT_TW

2.2.24 Pin SAVE

This pin is an open drain output with internal pull-up resistor to VIF.
In case of break-down of the bus voltage for more than typ. 1.5 ms (save condition) this pin delivers an active LOW signal to external host electronic.

Symbol	Parameter	Min	Max	Unit	Note
R_{PullUp}	Value of internal pull-up resistor to VIF	10	25	kΩ	
V_{max}	maximum voltage at SAVE pin		VIF + 0.5	V	
V_{OL}	output low voltage		0.2	V	1)
t_{FRG2}	Delay from VB+ break-down to SAVE= LOW (= debounce time of internal signal FRG2)	0.7	3	ms	Typ. 1.5 ms
t_f	fall time (90 % → 10 %)		100	ns	C_L = 150 pF 2)
1) I_{OL} of 1mA when VIF=1V; I_{OL} of 5mA when VIF ≥ 3V 2) Rise time determined by R_{PullUp}, C_L and VIF					

Table 24 Pin SAVE

2.2.25 Pin DIV

This input pin activates an internal 2:1 clock divider. If a 4.9152 MHz clock is used (quartz or external clock) then pin DIV must be connected to VDP. If an 2.4576 MHz clock is used (only external clock) then this pin must be connected to VB-.

Symbol	Parameter	Min	Max	Unit	Note
V_{IL}	voltage range for input low level	0	0.3 * VDP		
V_{IH}	voltage range for input high level	0.7 * VDP	1.0 * VDP		

Table 25 Pin DIV

3 Digitalpart

TP-UART 2+ is at the digital interface compatible with TP-UART. This means that the same drivers and stacks can be used without modification.

In addition TP-UART 2+ supports some additional useful services. These services reduce the necessary performance in the microcontroller.

3.1 Relationship to ISO-Reference-Model

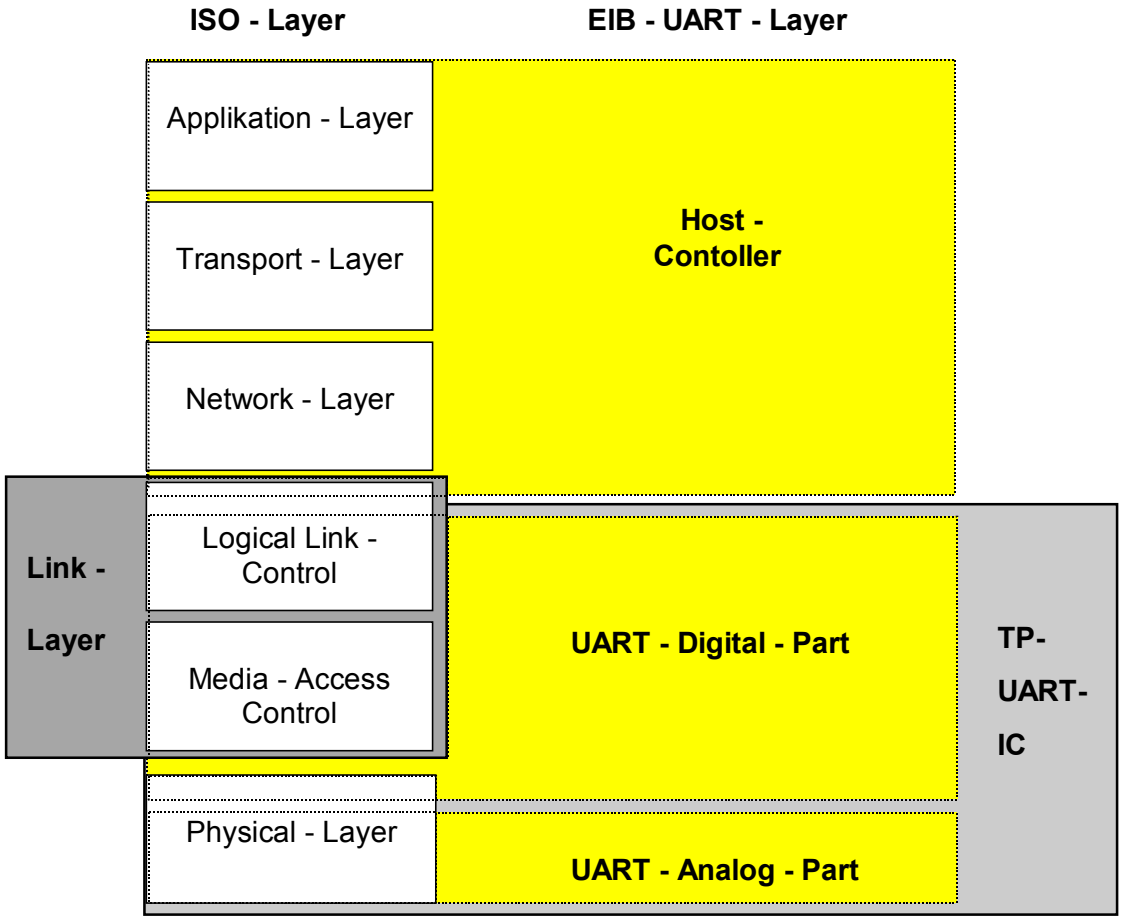

Fig. 1: ISO/ OSI Layer

Tasks of the Logical Link - Control in:
TP-UART: Checksum, Parity, Immediate Acknowledge, Repetition, Timing
Host - Controller : Checksum, Parity, Addressing, Length

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3.2 UART – Interface to host controller

3.2.1 Configuration and Timing

The TP-UART-IC has a full duplex UART-interface to transmit and receive KNX frames asynchronously. The baud-rate depends on the setting of BDS pin (115200 or 19200). The frame format consists of a start bit (=0), eight data bits (LSB first), an even parity bit and one stop bit (=1)

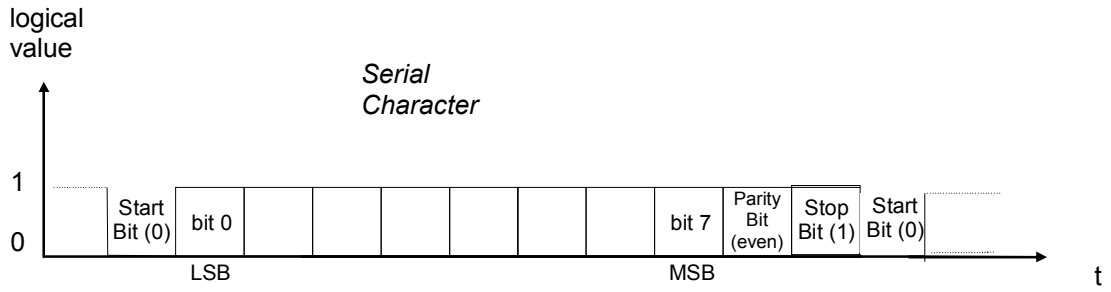

Fig. 2: UART Interface

The parity bit of every received byte from the host will be checked by the TP-UART. Errors will be reported to the host controller. Erroneous bytes (faulty parity) from EIB receiver will be checked too, but the host won't be informed. In those cases the host controller has to recognize the parity faults in the transmitted telegrams by its own. The UART receiver accepts frames up to a maximum baud rate deviation of 3%.

3.2.2 Resetbehavior

After connecting the operating voltage the TP-UART-IC generates an active reset (level 0 V) at pin RESn. This is valid for all modes. If Normal Mode is activated the following will happen at the UART-interface.
TxD will be 0 as long as there was no bus signal on the EIB for 40 Tbit (1 Tbit = 1/9600 s; Attention: The bittime of RxD/TxD depends on the adjusted baud rate at the UART-interface, for example 1/12 Tbit or 0,5 Tbit). This results in a complete time of 40 Tbit + 12 Tbit = 5,42 ms. Then TxD changes for 1 Tbit to 1 and following the service TP-UART-Reset.Indication is transmitted. This signal behavior on TxD appears after each reset.

3.2.3 UART-Protocol Definition

The protocol between TP-UART-IC and the application controller is a two wire protocol with software handshake. Each data byte transmitted to the TP-UART-IC is started with a control byte. Each data byte received on the EIB is transparently transmitted through the TP-UART-IC and is therefore started with the EIB control field. Additional Information from the TP-UART-IC is transmitted with an ESC code on the EIB control field. The host controller which is connected to the TP-UART-IC needs either to detect a receive time-out of 2 to 2,5 ms to detect an end of Packet or check the CRC16-CCITT.

3.2.3.1 Services to UART

The following Services are supported from the TP-UART-IC.

- U_Reset.request
- U_State.request
- U_ActivateBusmon
- U_AckInformation (Nack, Busy, Addressed)

- U_ProductID.request
- U_ActivateBusyMode
- U_ResetBusyMode
- U_MxRstCnt + Repetitions
- U_ActivateCRC
- U_Set_Address +PhysAddressHigh +PhysAddressLow
- U_L-Data Start + CTRL-Byte
- U_L-Data Continue (index) + Data-Byte
- U_L-Data-End + Checksum
- U_PollingState (Slotnumber) + PollAddrHigh + PollAddrlow + State

Uart-Control Field								Servicename	Hex		
7	6	5	4	3	2	1	0				
0	0	0	0	0	0	0	1	U_Reset.request	01		
0	0	0	0	0	0	1	0	U_State.request	02		
0	0	0	0	0	1	0	1	U_ActivateBusmon	05		
0	0	0	1	0	n	b	a	U_AckInformation	10-17	n,B,a:	Nack,Busy,Addressed
0	0	1	0	0	0	0	0	U_ProductID.request	20		
0	0	1	0	0	0	0	1	U_ActivateBusyMode	21		
0	0	1	0	0	0	1	0	U_ResetBusyMode	22		
0	0	1	0	0	1	0	0	U_MxRstCnt	24		
0	0	1	0	0	1	0	1	U_ActivateCRC	25		
0	0	1	0	1	0	0	0	U_SetAddress	28		
1	0	0	0	0	0	0	0	U_L_DataStart	80		
1	0	i	i	i	i	i	i	U_L_DataContinue	81-BE	i = Index	1 ... 62
0	1	l	l	l	l	l	l	U_L_DataEnd	47-7F	l = length	7 ... 63
1	1	1	0	s	s	s	s	U_PollingState	E0-EE	s= Slotnumber	0 ... 14

Fig. 3: Uart-Control Field

3.2.3.1.1 U_Reset.request-Service

Resets the TP-UART-IC to the initial state and clears all buffers. At start-up the TP-UART waits for a bus free-time-out before sending a U_Reset.indication-Service to the host. To be sure that the TP-UART is reset after power up the host shall wait for 50 ms after reset signal is high and then send the U_Reset.request-Service.

UART-Controlfield (01_{hex})							
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	1

Fig. 4: U_Reset.request-Service

3.2.3.1.2 U_State.request-Service

Requests the internal communication state from the TP-UART-IC. The TP-UART-IC answers with the Communicationstate.

UART-Controlfield (02_{hex})							
7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	0

Fig. 5: U_State.request-Service

3.2.3.1.3 U_ActivateBusmon-Service

Activates the busmonitormode. That means that each byte which is received on the EIB is sent through the TP-UART-IC including illegal Control-bytes and not used Immediate ACK. The TP-UART-IC is absolutely quiet on the EIB. The busmonitormode can only be left by using the U_Reset.request-Service.

UART-Controlfield (05_{hex})							
7	6	5	4	3	2	1	0
0	0	0	0	0	1	0	1

Fig. 6: U_ActivateBusmon

3.2.3.1.4 U_ProductID.request

Requests the internal TP-UART-IC product identifier. The TP-UART-IC answers with the U_ProductID.response service

UART-Controlfield (20_{hex})							
7	6	5	4	3	2	1	0
0	0	1	0	0	0	0	0

Fig. 7: U_ProductID.request

3.2.3.1.5 U_ActivateBusyMode

If the host controller is temporarily not able to receive telegrams from the bus (e.g. due to no code execution during flash erase), the TP-UART should reject frames from the bus with BUSY acknowledges. The service activates the BUSY mode in the TP-UART for a fix period of 700 ms (+/- 10ms). This means that all addressed telegrams (TP-UART has internally the "addressed" bit set) are acknowledged with Busy.

Note: physical addressed frames which do not correspond with the TP-UART address will never be acknowledged with BUSY!

All received telegrams are sent byte by byte from the TP-UART to the host as before. If the host confirms a frame with the U_Ackinfo service (ACK, NACK or BUSY) the BusyMode will be deactivated. After reset the BusyMode will be also deactivated.

UART-Controlfield (21_{hex})							
7	6	5	4	3	2	1	0
0	0	1	0	0	0	0	1

Fig. 8: U_ActivateBusyMode

3.2.3.1.6 U_ResetBusyMode

The service U_ResetBusyMode deactivates immediately the BUSY mode in the TP-UART. All addressed telegrams are answered according to the intern address flags. The host shall synchronize its receiver before sending the U_ResetBusyMode.

UART-Controlfield (22_{hex})							
7	6	5	4	3	2	1	0
0	0	0	1	0	0	1	0

Fig. 9: U_ResetBusyMode

3.2.3.1.7 U_SetAddress

This service configures the physical address of the TP-UART. If this service is repeatedly sent (e.g. the physical address changes), the new address will be active in the TP-UART after reception of the complete U_SetAddress service and when no Layer 2 frame is currently received from the EIB. If the address is set a complete address evaluation in the TP-UART is activated (group-addressed telegrams are now generally confirmed).
Note: The TP-UART does not evaluate the received EIB telegrams which were sent itself.
After reset the address evaluation is deactivated again.

UART-Controlfield (28_{hex})							
7	6	5	4	3	2	1	0
0	0	1	0	1	0	0	0

physical address high								physical address low							
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
a	a	a	a	l	l	l	l	d	d	d	d	d	d	d	d

Fig. 10: U_SetAddress

The TP-UART analyzes after setting the physical address independently of the host controller all telegrams and evaluates the destination address. If addressed then the IACK generation takes place. The TP-UART analyses for this reasons the different frame formats (standard frame and extended frame format according to the KNX standard).

- Frameformat **Standard**:

Octet 0	...	Octet 3	Octet 4	Octet 5	...
Ctrlbyte **1**0R1cc00	...	High byte destaddress	Low byte destaddress	NPCI **A**xxx xxxx	...

- Frameformat **Extended**:

Octet 0	Octet 1		Octet 4	Octet 5	...
Ctrlbyte **0**0R1cc00	extCtrlbyte **A**xxx xxxx		High byte destaddress	Low byte destaddress	...

a) group (multicast) or broadcast addresses
if (**A** == 1) then group addressed
=> “addressed”

b) physical addressed (point to point)
if (**A** == 0) then physical addressed
=> if (destination address == physical address of TP-UART)
=> “addressed”

If the TP-UART is “addressed” and no error occurs then the TP-UART sends an IACK. If the TP-UART is “addressed” and an error occurs (parity or checksum error) then it generates an INACK.

Note:
Also during activated address evaluation the host is able to manipulate the IACK generation of the TP-UART by sending the U_AckInformation service.

3.2.3.1.8 U_AckInformation-Service

The U_AckInformation-Service is only sent to the TP-UART if a host controller wants to check the destination address itself. This service is sent by the host after the address evaluation and must be sent latest 2,8 ms after receiving the address type octet of an addressed frame. The Nack-/ Busy-/ Addr-Bits sets internal flags in the TP-UART. The NACK flag is set by the TP-UART itself if it is detecting any frame error.
If the TP-UART receives this service and the addressed bit is set it will generate a ACK, NACK or BUSY-frame on the EIB depending on the settings of the NACK/busy-flags.

UART-Controlfield							
7	6	5	4	3	2	1	0
0	0	0	1	0	x	x	x
AckInformation					Nack	Busy	Addr

Fig. 11: U_AckInfo-Service

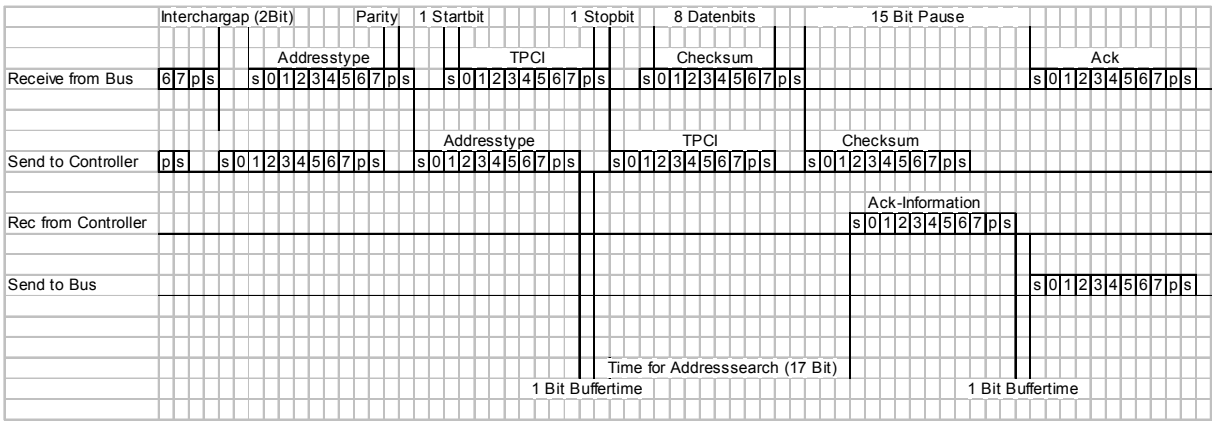

Fig. 12: Timing for send U_AckInfo(e.g. 19200 Baud)

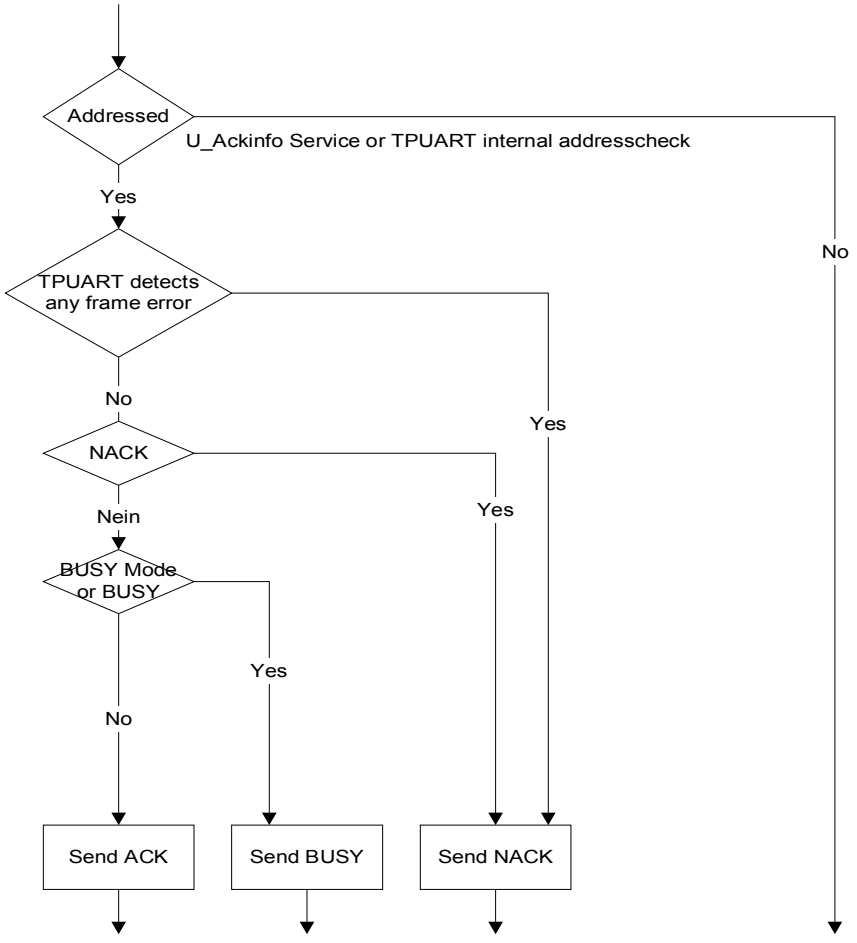

Fig. 13: Ack / Nack / Busy Generation of the TP-UART

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3.2.3.1.9 U_L_Data-Services

The U_L_Data-Services are used to transfer the complete EIB-Linklayer-Frame (L_Data.request and L_PollData.request) to the TP-UART.

If the host sends a second frame (the first frame buffer is yet active) the TP-UART rejects this and reports it with a Status.indication (PE bit set).

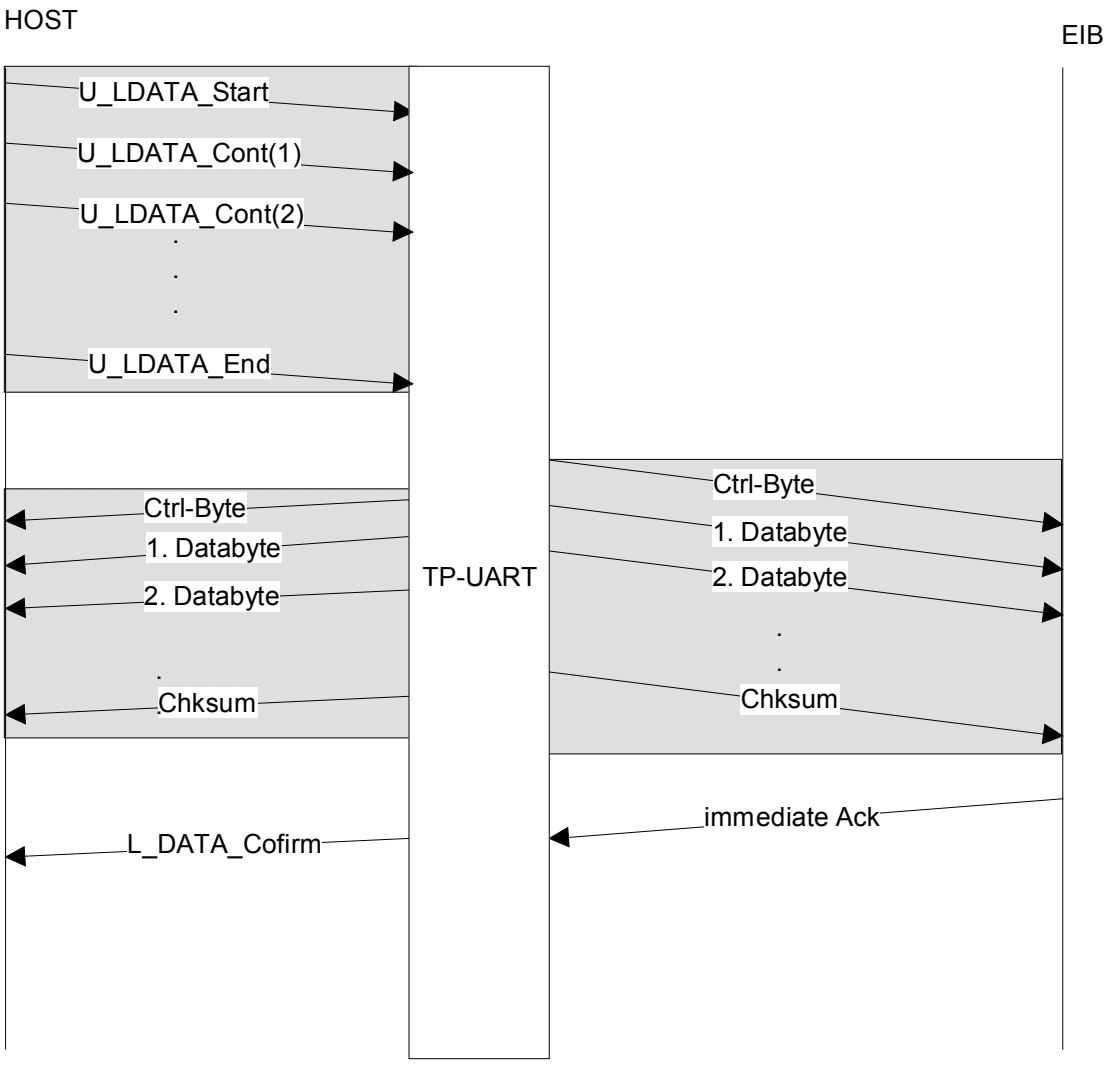


Fig. 14: TP-UART send telegram

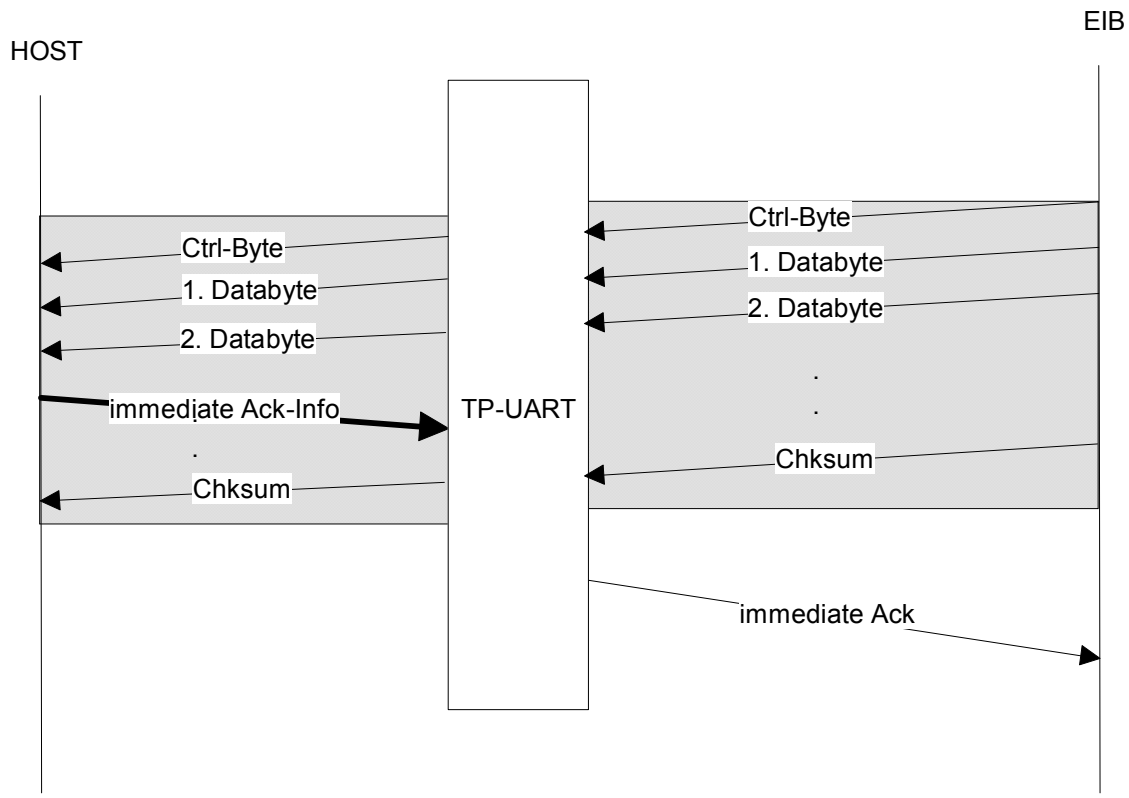


Fig. 15: TP-UART receive telegram

3.2.3.1.9.1 U_L_DataStart-Service

The U_L_DataStart-Service initialize the TP-UART-IC to receive a complete EIB-Linklayer-Frame from the host. As additional data the EIB-Control-byte is transmitted which is the control field of the L_Data-frame or L_Polldata-frame. If the repetition flag in the control byte is just cleared the TP-UART transmits the frame only once time with repetition flag set.

UART-Controlfield (80_{hex})								Additional Information							
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
1	0	0	0	0	0	0	0	F	F	R	1	c	c	0	0
L-Data			Data-Index 00 = Start					EIB-Controlfield							

Fig. 16: L_DataStart Service

FF = Frame Format
- 10 Standard Length L_DATA service
- 00 extended L_DATA service
- 11 L_POLLDATA service

R = Repeatflag (on the EIB 1 = not repeated, 0 = repeated)
- 1 = repeat the telegram on the EIB (see U_MxRstCnt service, default 3 times)
  send first time with repeatflag = 1 and repeat with repeatflag = 0
- 0 = don't repeat the telegram on the EIB; send only one time with repeatflag = 1

cc = class

control field FFR1 cc00	**data link frame type**	**class**	**repeat flag**
FFR1 0000	L_DATA request	system	set by TP-UART
FFR1 1000	L_DATA request	alarm	set by TP-UART
FFR1 0100	L_DATA request	high	set by TP-UART
FFR1 1100	L_DATA request	normal	set by TP-UART
1111 0000	L_POLLDATA request	system priority	= 1

Fig. 17: Legal EIB-Controlfield

3.2.3.1.9.2 U_L_DataContinue-Service

The U_L_DataContinue-Service transmits one byte of the contents of an EIB-L_Data-Frame to the TP-UART. The data-index starts with 1 and the maximum value is 62 depending on the length of the frame.

UART-Controlfield								Additional Information							
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
1	0	i	i	i	i	i	i	d	d	d	d	d	d	d	d
L-Data		Data-Index (1 – 62)						EIB-Data Byte for L-Data-Frame							

Fig. 18: U_L_DataContinue-Service

3.2.3.1.9.3 U_L_DataEnd-Service

The U_L_DataEnd-Service marks the end of the transmission of the EIB-Frame. After receiving this service the TP-UART checks the checksum and if correct the transmission starts on the EIB else the UART returns a state-indication with Receive-Errorflag is set.

UART-Controlfield(80_{hex})								Additional Information							
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
0	1	l	l	l	l	l	l	c	c	c	c	c	c	c	c
L-Data		Length (7 – 63)						Checksum							

Fig. 19: U_L_DataEnd-Service

3.2.3.1.9.4 U_MxRstCnt

This service adjusts the maximum number of repetitions on bus after a frame has not been acknowledged with IACK. Values from 0 to 7 are separately adjustable for BUSY or INACK. No acknowledge will be handled as INACK. If the host clears the repetition flag in the U_L_DataStart service always no repetitions will be sent.
After Reset 3 repetitions are active.

UART-Controlfield (24_{hex})								MxRstCnt							
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
0	0	1	0	0	1	0	0	c	c	c	0	0	c	c	c
								Busy Cnt					Nack Cnt		

Fig. 20:U_MxRstCnt

3.2.3.1.9.5 U_ActivateCRC

This service activates a 16 bit CRC calculation for every received Layer 2 Service from the bus (except when the TP-UART is Polling Slave or the busmonitormode is active). However the CRC calculation only becomes active at the host speed of 19200 Baud.

The TP-UART calculates over the complete received telegram (including the Layer 2 checksum) a CRC16-CCITT with the following parameters:

- Width= 16 bit
- Truncated polynomial = 1021hex
- init value = FFFFh
- I/O not reflected
- no xor on output CRC
- Test string „123456789“ is 0xE5CC

and adds it to the receiving frame (sending order is highbyte then lowbyte).

After Reset CRC calculation is disabled.

UART-Controlfield (25_{hex})							
7	6	5	4	3	2	1	0
0	0	1	0	0	1	0	1

Fig. 21: U_ActivateCRC

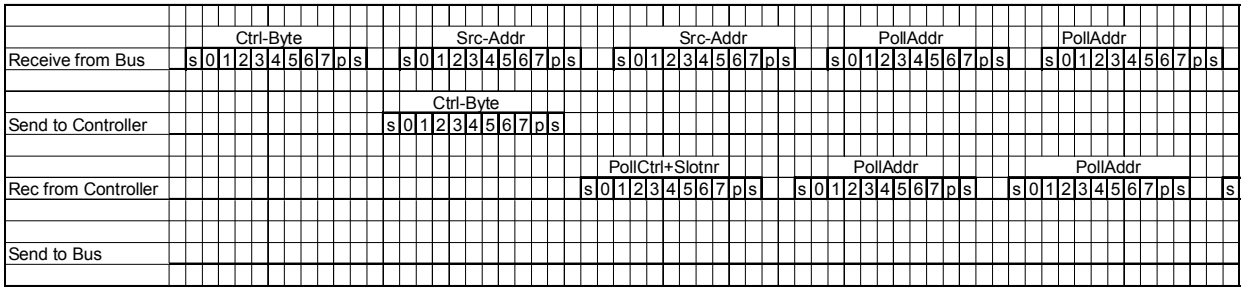
3.2.3.1.9.6 U_PollingState

This service must be send to the TP-UART if an Pollingframe-Ctrlbyte is received. If the TP-UART detects a collision during sending the slave slot to the EIB the TP-UART generates a State indication with the Slave Collisionflag set.

UART-Controlfield								Polling Address high							
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
1	1	1	0	s	s	s	s	c	c	c	c	c	c	c	c
				Slotnumber											

Polling Address low								Pollingstate							
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c

Fig. 22: U_PollingState-Service



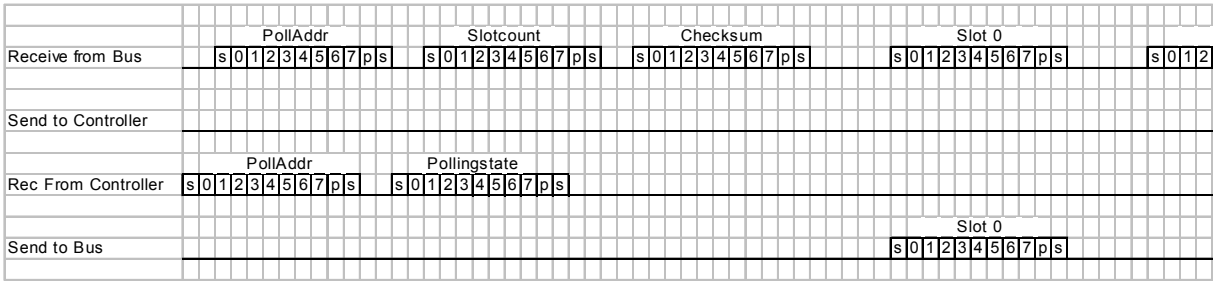
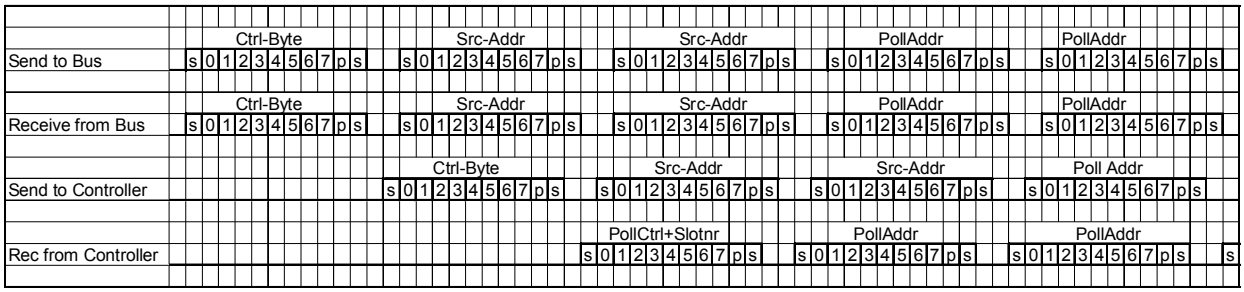


Fig. 23: Timing for U_PollingState-Service (Host is slave)



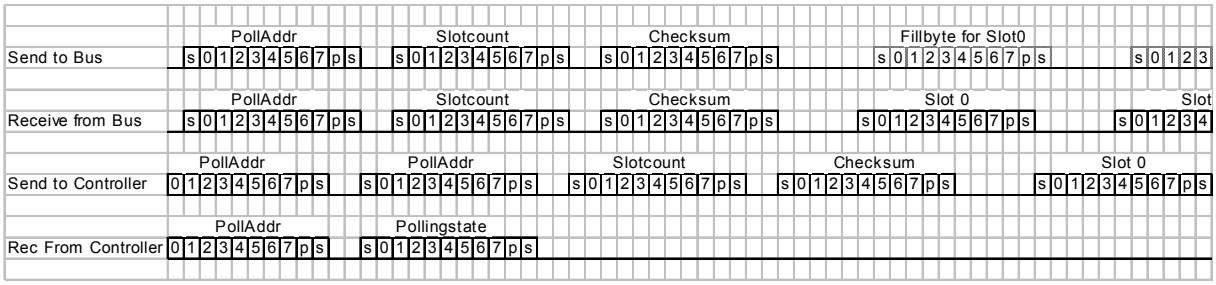


Fig. 24: Timing for U_PollingState-Service for a Master

3.2.3.1.9.7 Services from UART

The first character of each service sent to the host is the control field. The control field contains the information about the TP-UART-Service. There are 3 types of services sent to the host, the EIB-Layer-2-Services, immediate acknowledge services and the special TP-UART-Services. The EIB-Layer-2-Services contains information about its class and a flag containing the information whether the LPDU is a repeated one. The immediate acknowledge services are only sent in busmonitormode and includes informations about successful sending. The TP-UART-Services are to inform the host about the communicationstate or to reset the communication.

Control Field							
7	6	5	4	3	2	1	0

Layer-2 Services

		repeat flag		class	class			
1	0	r	1	c1	c0	0	0	L_DATA.req
0	0	r	1	c1	c0	0	0	L_EXT_DATA.req
1	1	1	1	0	0	0	0	L_POLLDATA.req

Immediate Acknowledge Services

1	1	0	0	1	1	0	0	Acknowledge frame
0	0	0	0	1	1	0	0	NotAcknowledge frame
1	1	0	0	0	0	0	0	Busy frame

TP-UART-Control-Services

0	0	0	0	0	0	1	1	Reset-Indication
x	x	x	x	x	x	x	x	ProductID.response
x	x	x	x	x	1	1	1	State.response/indication
x	0	0	0	1	0	1	1	L_DATA.confirm

repeat flag = 0: repeated L_DATA frame

c1	c0	
0	0	system priority
1	0	urgent priority
0	1	normal priority
1	1	low priority

x = 1 Positive Confirm
x = 0 Negative Confirm

Fig. 25: Control Field

3.2.3.1.10 Layer-2 Services

The Layer-2 Services includes all standard EIB-Linklayer Services. The Controlfields are followed by the data of the EIB-Frame. All bytes received on the EIB are immediately sent to the host. The host either has to detect an end of packet timeout by supervising the EOP gap of 2 - 2,5 ms or check the end of frame by calculating the CCITT CRC (must be enabled by the U_ActivateCRC service).

control field FFR1 cc00	**Hexadecimal**	**data link frame type**	**class**	**repeat flag** (0 = repeated)
FF11 0000	$30/B0_{Hex}$	L_DATA request	system	not repeated
FF01 0000	$10/90_{Hex}$	L_DATA request	system	repeated
FF11 1000	$38/B8_{Hex}$	L_DATA request	urgent	not repeated
FF01 1000	$18/98_{Hex}$	L_DATA request	urgent	repeated
FF11 0100	$34/B4_{Hex}$	L_DATA request	normal	not repeated
FF01 0100	$14/94_{Hex}$	L_DATA request	normal	repeated
FF11 1100	$3C/BC_{Hex}$	L_DATA request	low	not repeated
FF01 1100	$1C/9C_{Hex}$	L_DATA request	low	repeated
1111 0000	$F0_{Hex}$	L_POLLDATA request	system	

Fig. 26: Controlfield for Layer 2 Services

The Frameformat 01 is not supported.

For a complete description of the Linklayer service see the KNX Standard.

Each L_Data-request is transmitted completely to the Host. From a L_PollData-request only the Controlbyte is transmitted to the host if the TP-UART is a polling slave. If the TP-UART is polling master the complete polling frame is transmitted to the host as well if a collision is detected during sending the polling master frame.

If the 16 bit CRC calculation is enabled (see U_ActivateCRC , the host baud rate have to be 19200) then the Linklayer service follows a 16 bit CRC (order Highbyte, Lowbyte). The timing is fix for both supported baudrates. The high byte of the CRC is sent 6.5 Tbit after the last received octet from bus (calculated after stopbit) and the low byte is sent immediately afterwards.

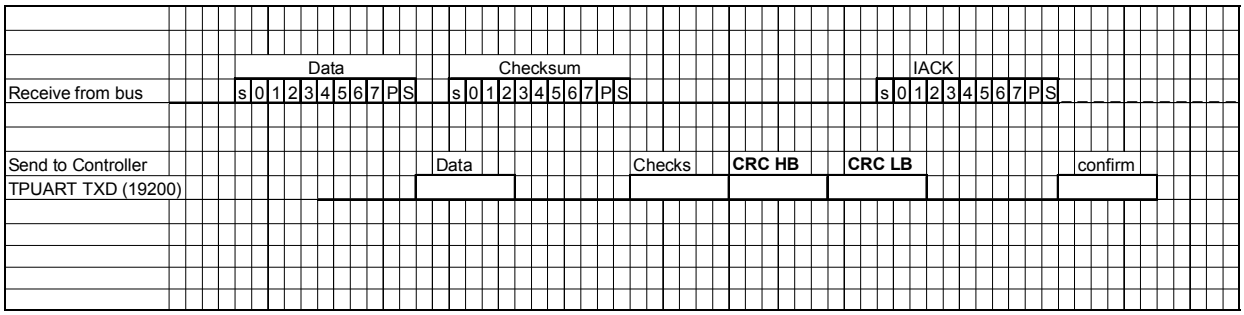


Fig. 27: Timing for CRC 16 bit

3.2.3.1.11 Acknowledge Services

Acknowledge services are only transmitted to the host in busmonitormode.
Note: In busmonitormode each received byte on the EIB is sent through the TP-UART-IC including illegal control bytes and not used Immediate ACK. The TP-UART-IC is in this mode absolutely quiet on the EIB.

The short acknowledgement frame format consists of 15 bit times idle time followed by a single character which is used to acknowledge an L_Data.req frame. The following Figure shows the corresponding codes of the short acknowledgement.

Octet 0								
Short ACK								
8	7	6	5	4	3	2	1	
1	1	0	0	1	1	0	0	ACK
0	0	0	0	1	1	0	0	NAK
1	1	0	0	0	0	0	0	BUSY

Fig. 28: Short Acknowledgement Frame Format

3.2.3.1.12 TP-UART-Control Services

The TP-UART-Control service exist only on this interface. They are to reset the communication or to inform the host about the actual state.

3.2.3.1.12.1 TP-UART-Reset.indication Service

The Reset.indication service is sent after each reset if 40 bit-times line idle was detected.

TP-UART-Controlfield							
7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	1

Fig. 29: TP-UART-Reset.indication-Service

3.2.3.1.12.2 TP-UART-ProductID.response Service

The ProductIdentifier.response service is sent if a U_ProductID.request service was received from the host.
Release a: 0100 0001

TP-UART-Controlfield							
7	6	5	4	3	2	1	0
i	i	i	r	r	r	r	r
Product ID			revision number				

Fig. 30: TP-UART-ProductID.response-Service

3.2.3.1.12.3 TP-UART-State.indication/response Service

The TP-UART-State.response-service is sent if an U_State.request-Service was received from the host. If the TP-UART is too hot (over-temperature), the TW-bit has the value 1. In case of Slave Collision, Receive Error, Checksum Error or Protocol Error or Recognition Over-Temperature or Recognition Leaving-Over-Temperature the TP-UART sends a State.indication-Service.

TP-UART-Controlfield							
7	6	5	4	3	2	1	0
SC	RE	TE	PE	TW	1	1	1

Fig. 31: TP-UART-StateIndication/Response-Service
SC = Slave Collision
RE = Receive Error (Checksum, Parity or Biterror)
TE = Transmitter Error (send 0 receive 1)
PE = Protocol Error e.g. illegal controlbyte
TW = Temperature Warning

Attention: A received L-Data-Frame can follow the State indication without any delay.

3.2.3.1.12.4 TP-UART-L_Data.confirm Service

The L_DATA.confirm service is transmitted to the host if an acknowledge was received or if the last repetition is transmitted and no acknowledge was received.

TP-UART-Controlfield							
7	6	5	4	3	2	1	0
x	0	0	0	1	0	1	1

Fig. 32: TP-UART-L_DATA.confirm-Service
X = 1 The transmission of the L_DATA-frame was successful
X = 0 The transmission of the L_DATA-frame was not successful

4 Mechanical Specification

4.1 Package

Package type: Punched QFN36 6x6x0.9mm

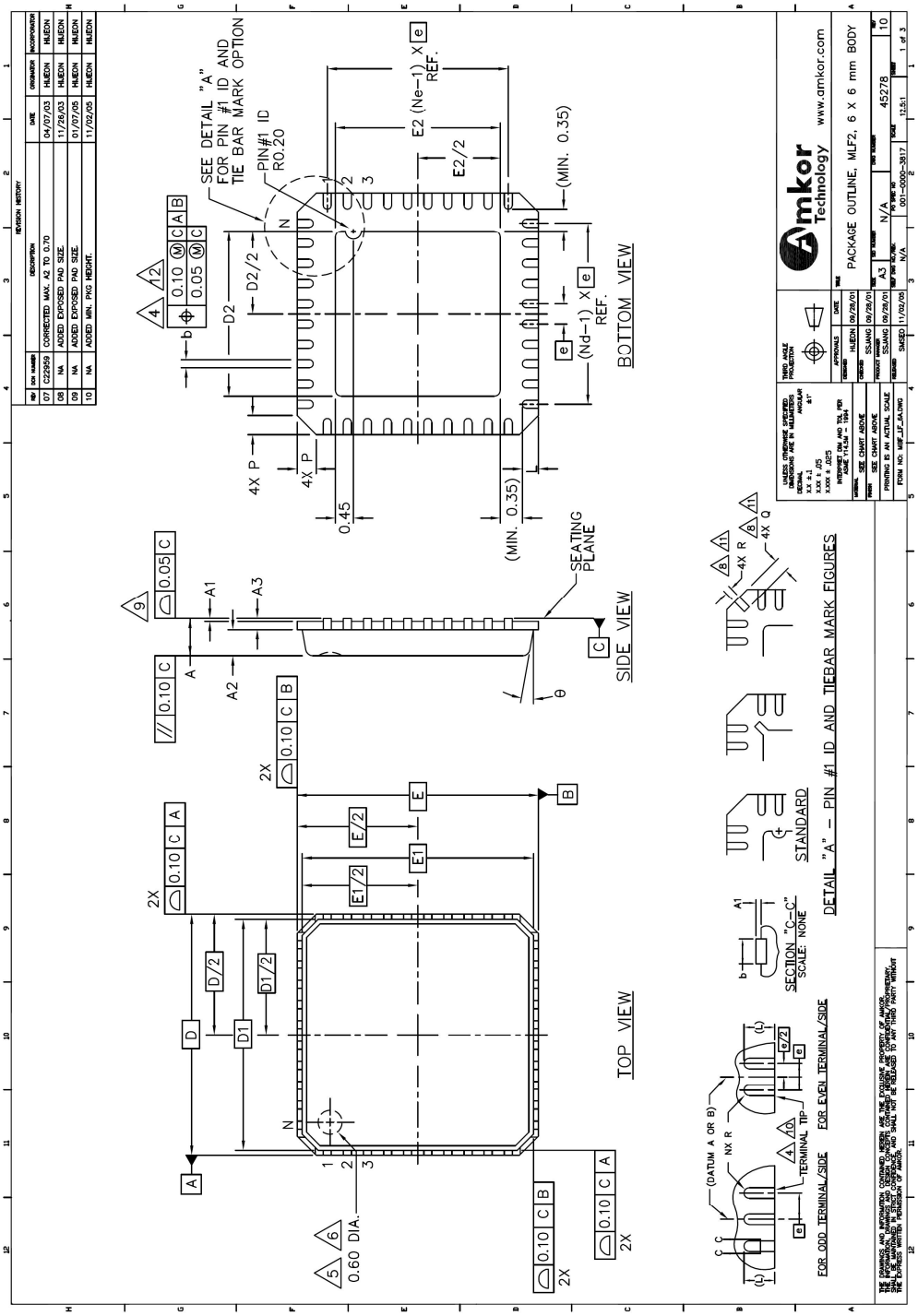


Figure 4 Package outline, Punched QFN 6x6x0.9mm 36LD 0.5mm Lead Pitch

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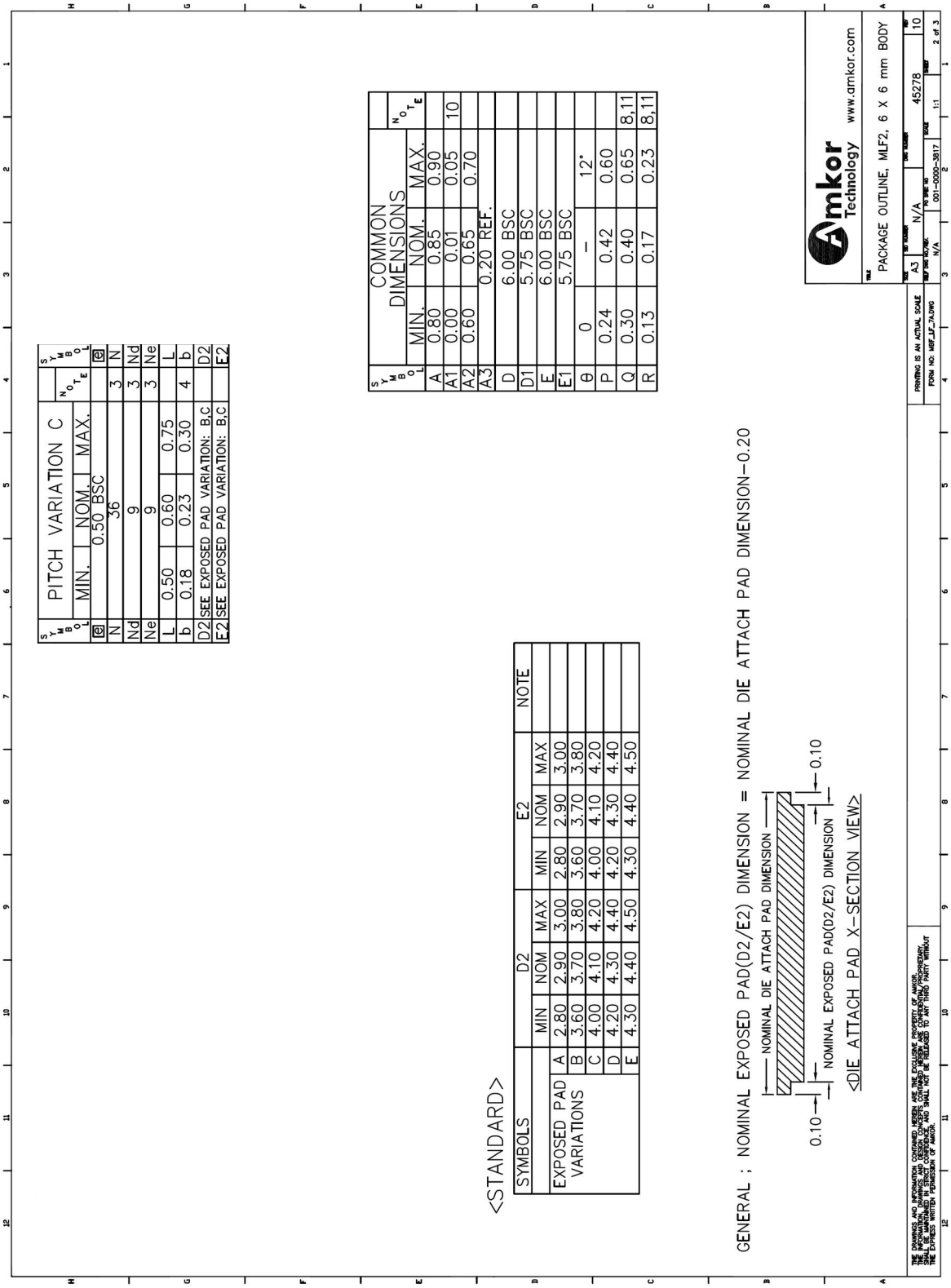

Figure 5 Package dimensions, Punched QFN 6x6x0.9mm 36LD 0.5mm Lead Pitch **(Variant C)**

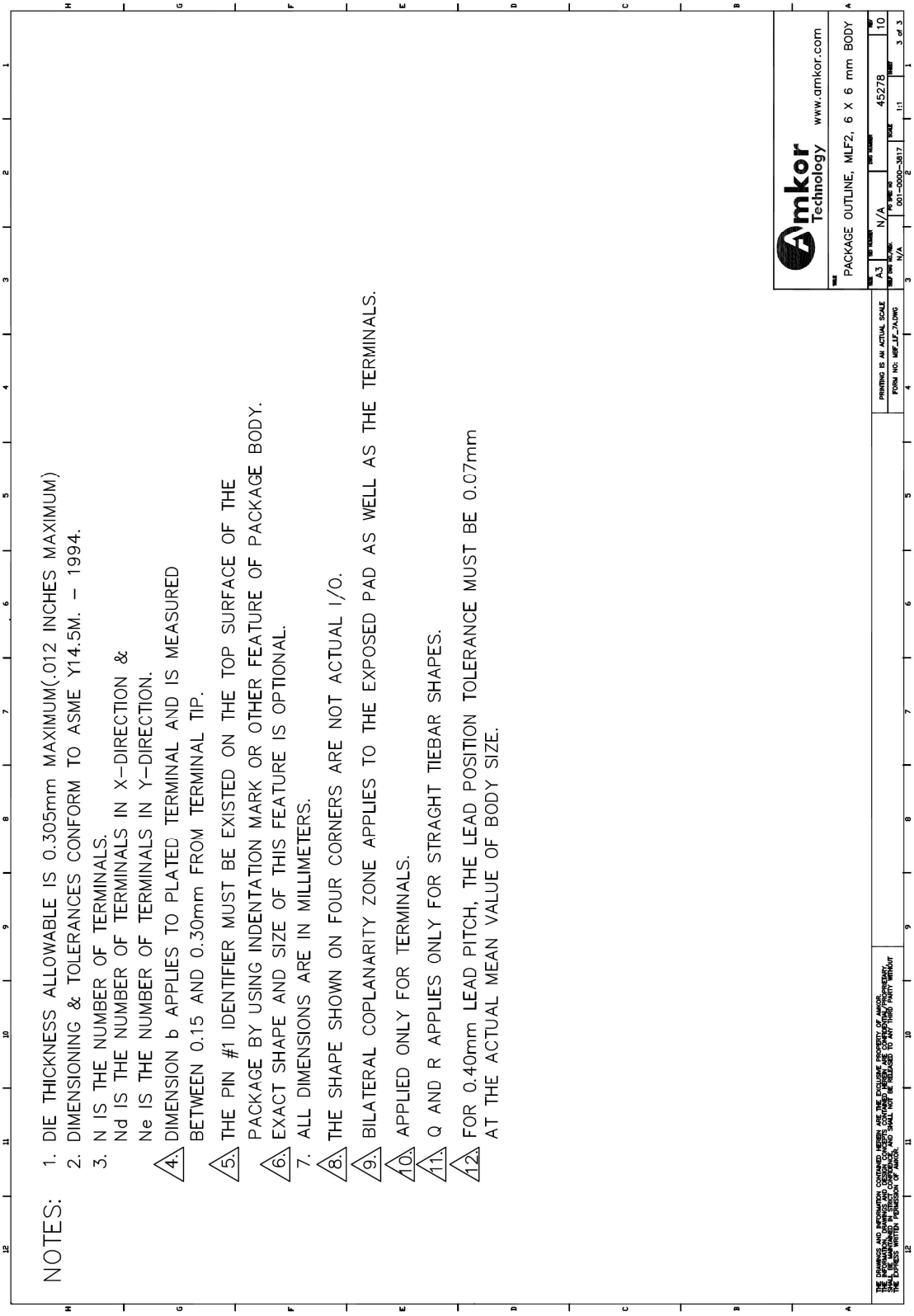

Figure 6 Package notes, Punched QFN 6x6x0.9mm 36LD 0.5mm Lead Pitch

5 Tape and Reel Packing

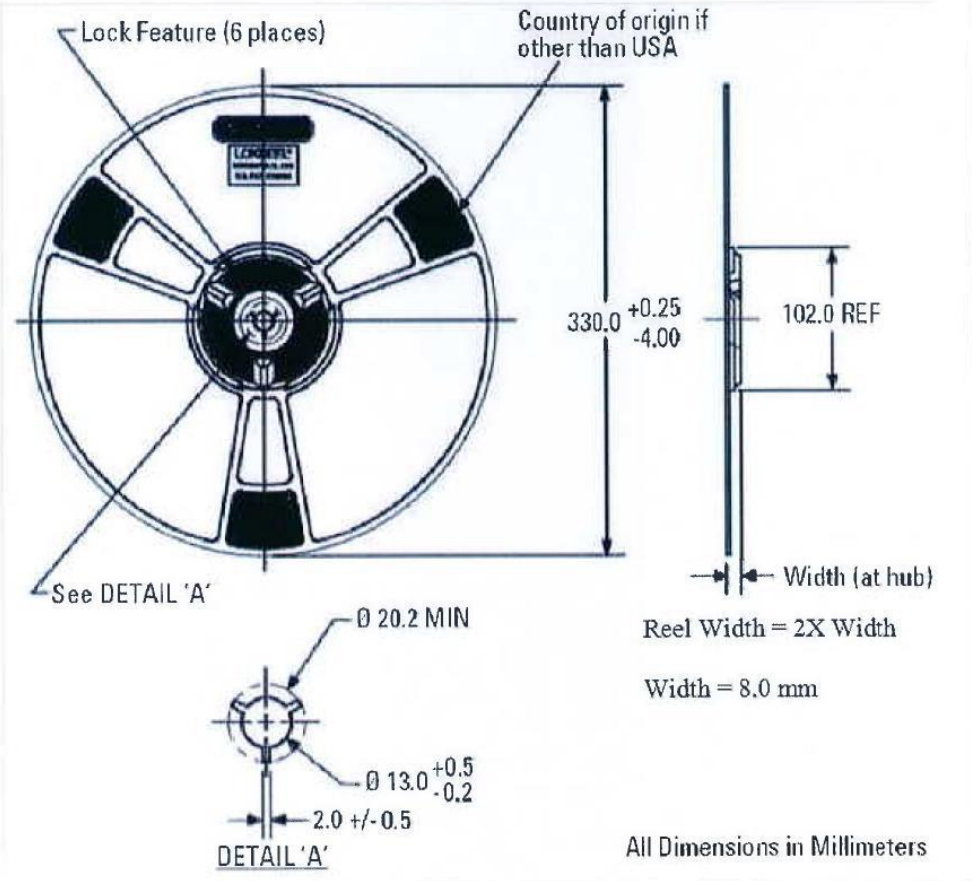

Figure 7 Tape and Reel Packing 1

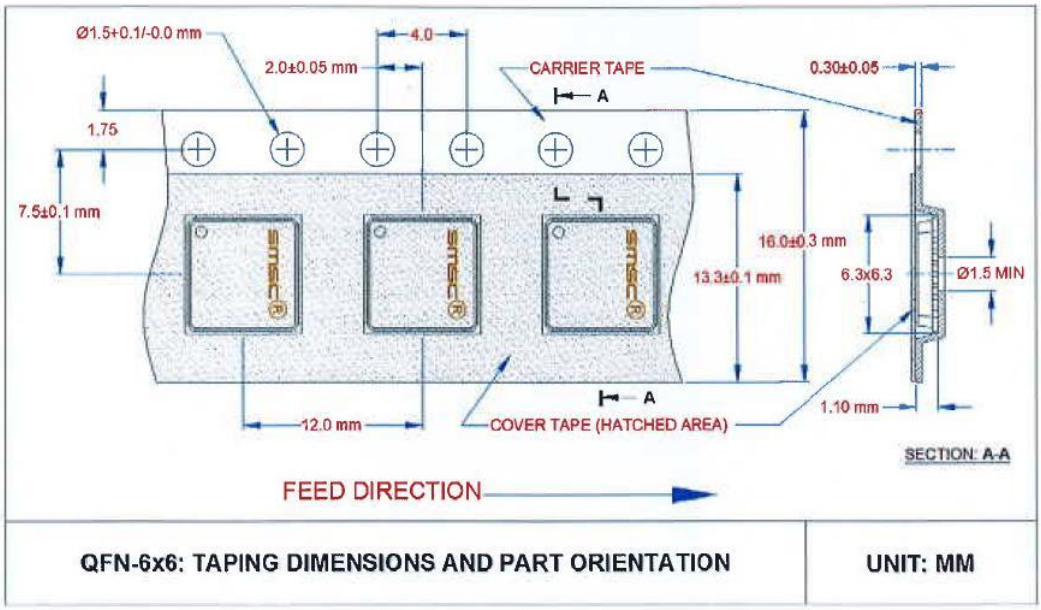

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Figure 8 Tape and Reel Packing 2

6 Soldering Profile

Symbol	Parameter	Value	Unit	Note
T_C	Classification Temperature	260	°C	
T_{smin}	Temperature min	150	°C	Preheat/Soak
T_{smax}	Temperature max	200	°C	Preheat/Soak
t_S	Time	60-120	s	T_{smin} to T_{smax}
T_L to T_P	Ramp-up rate (T_L to T_P)	≤ 3	°C/s	
T_L	Liquidous Temperature	217	°C	
t_L	Time (t_L) maintained above T_L	60-150	s	
T_P	Peak package body temperature	260	°C	
t_P	Time (t_P) within 5 °C of the specified classification temperature (T_C), see Figure 5-1	30	s	
T_P to T_L	Ramp-down rate (T_P to T_L)	≤ 6	°C/s	
t_{25} to t_P	Time 25 °C to peak temperature	≤ 8	min	

Table 26 Soldering Profile

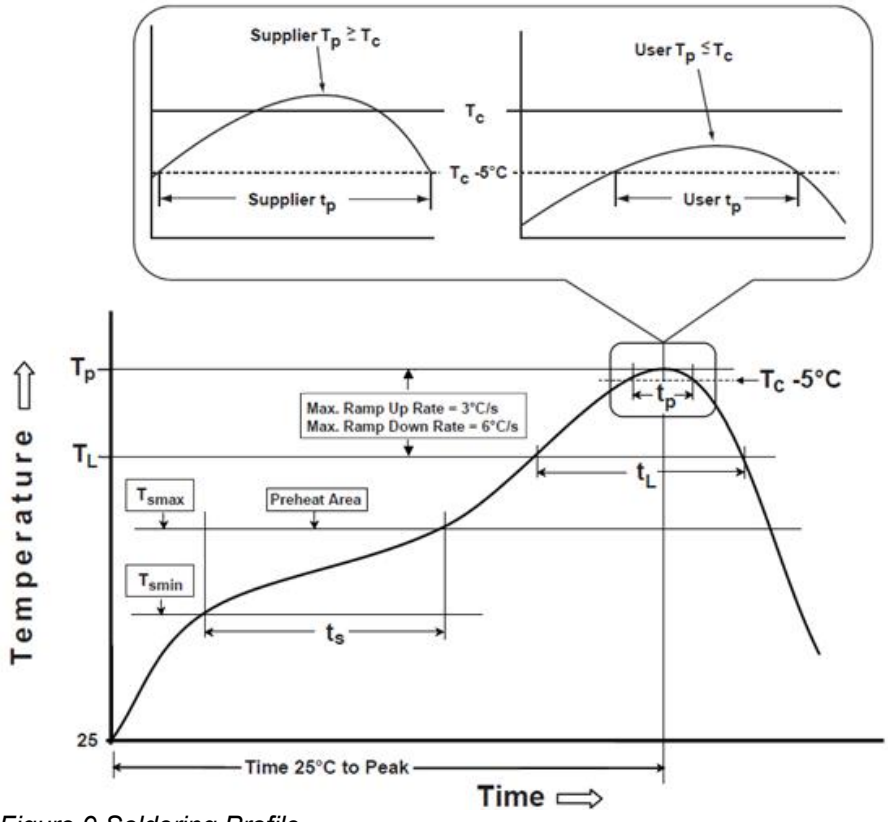


Figure 9 Soldering Profile

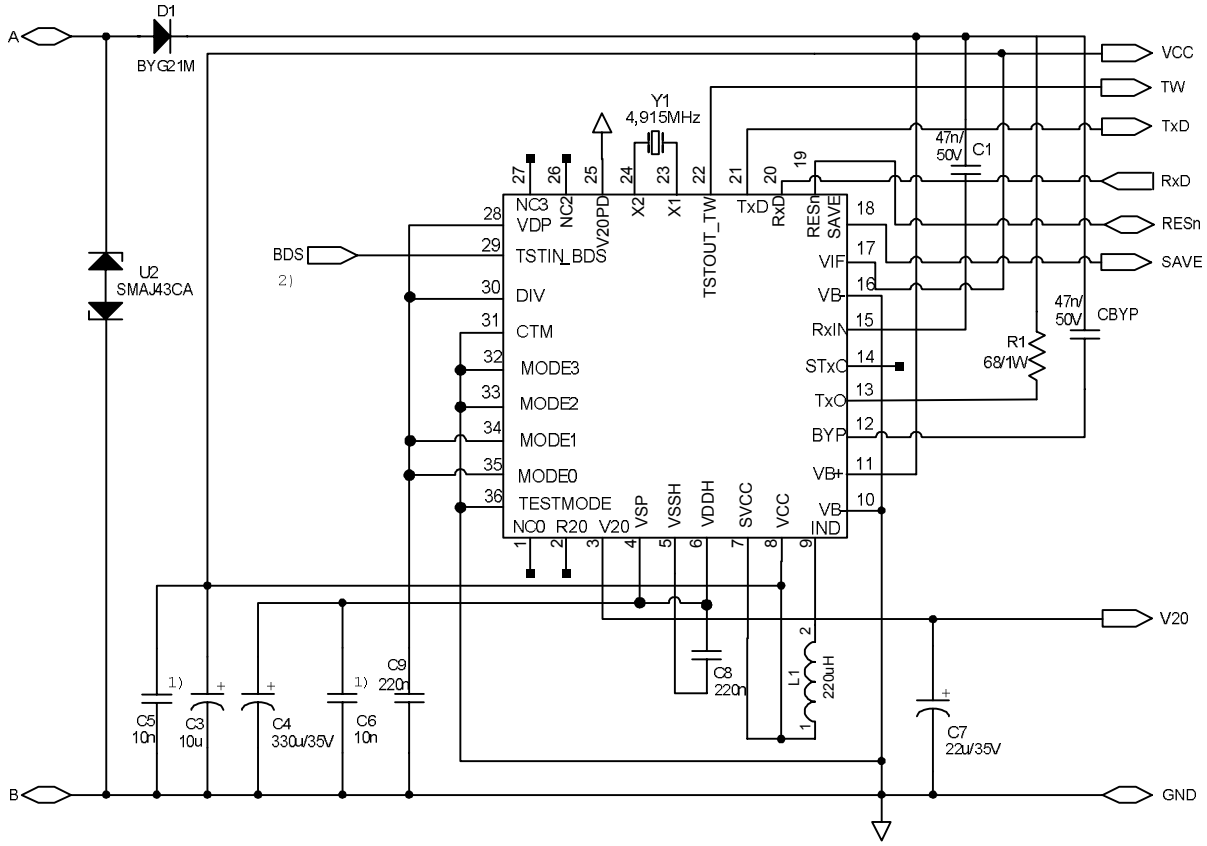
Moisture Sensitivity Level:	3
Maximum number of running a reflow profile:	3
Plating:	pure tin (matte tin)

7 Appendix

7.1 Typical Application Circuits

In all the applications circuits shown below a default value of VCC=5V is used.

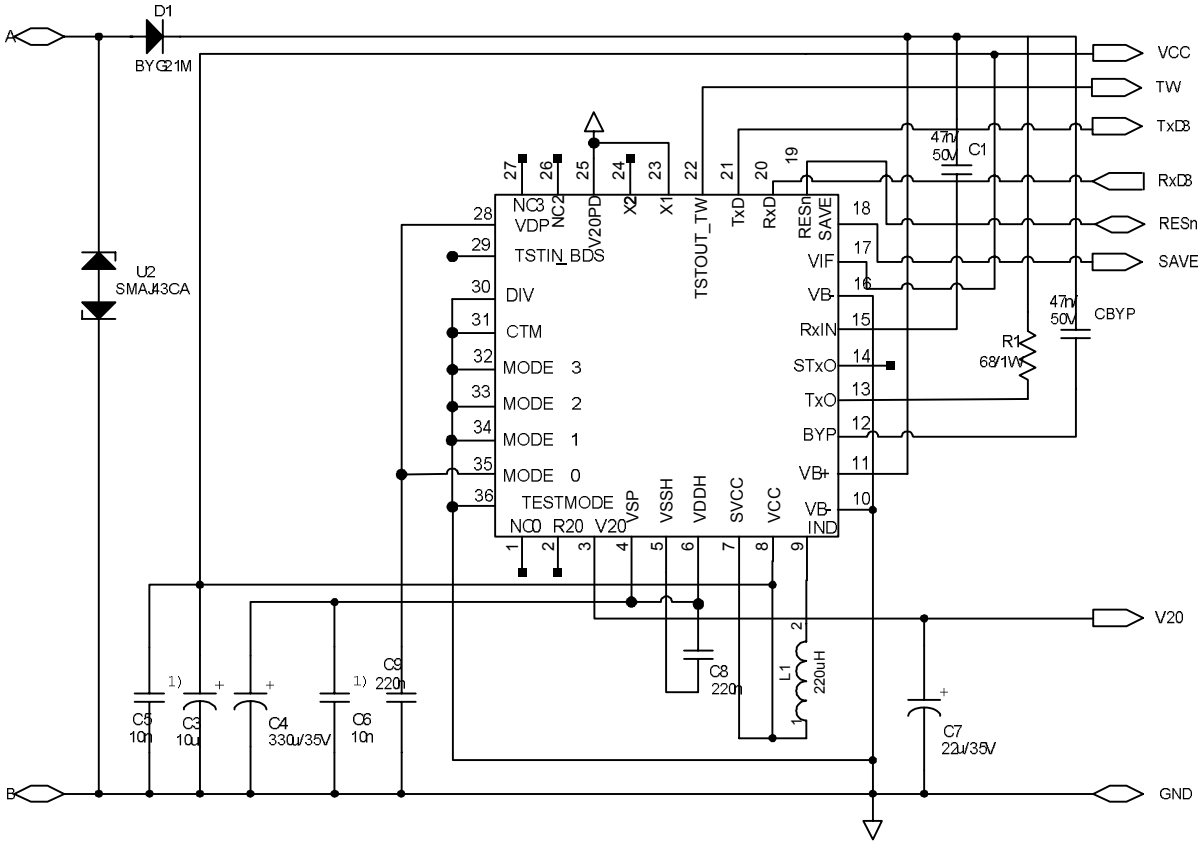
7.1.1 Mode of Operation – Normal



1. recommended (close to Pins VDDH and VCC)
2. BDS shall not float

Figure 10 Mode of Operation – Normal

7.1.2 Mode of Operation – Analog



3. recommended (close to Pins VDDH and VCC)
4. The maximum average power dissipation of the transmitting resistance R1 of 1 W is valid for an active telegram rate of 50 %.

Figure 11 Mode of Operation – Analog

7.2 Layout Guidelines

The guidelines related to Figure 10 Mode of Operation – Normal.

Nr.	Component	Layout Guidelines	Priority
1	C9	As close as possible to VDP and GND	1
2	C8	As close as possible to VSSH and VDDH	2
3	L1	As close as possible to IND and GND	2
4	C5	As close as possible to VCC and GND	2

5	C3	As close as possible to VCC and GND	3
6	CBYP	As close as possible to BYP and VB+	2
7	C6	As close as possible to VSP and GND	2
8	Y1	As close as possible to X1 and X2 Embed Y1 (crystal) and its connections on the component side in GND Place on next layer below Y1 a GND area.	1
9	TP-UART 2+	Ground plane on component side and below TP-UART 2+ has to be designed. Four vias are necessary.	1

Table 27 Layout Guidelines

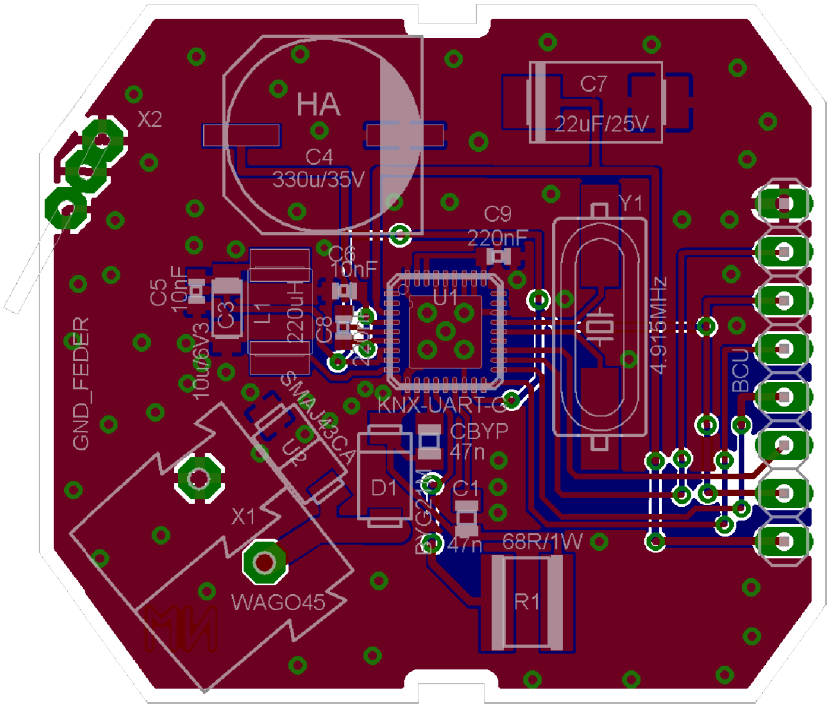


Figure 12 Layout Top-/Bottom View

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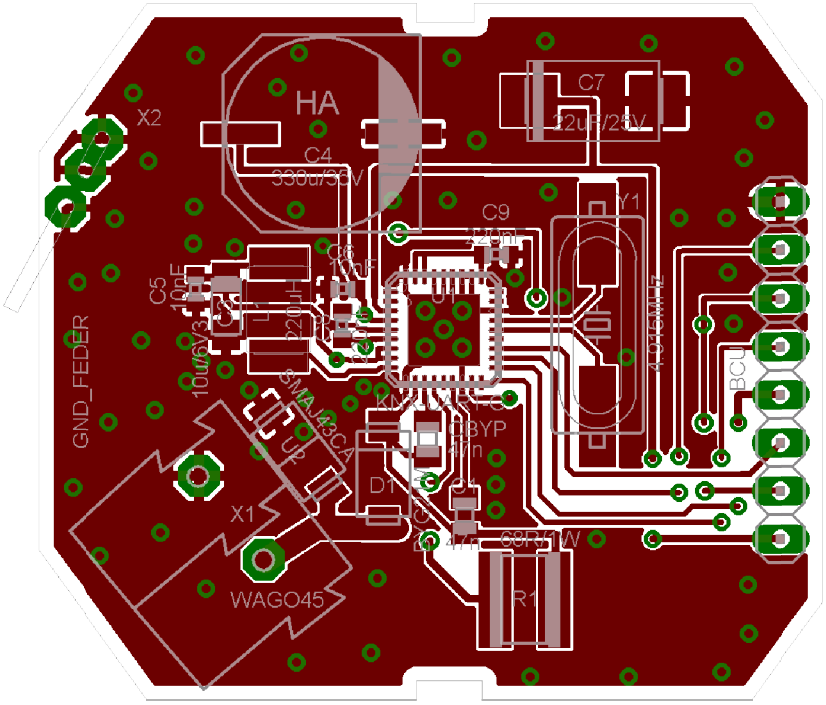

Figure 13 Layout Topview

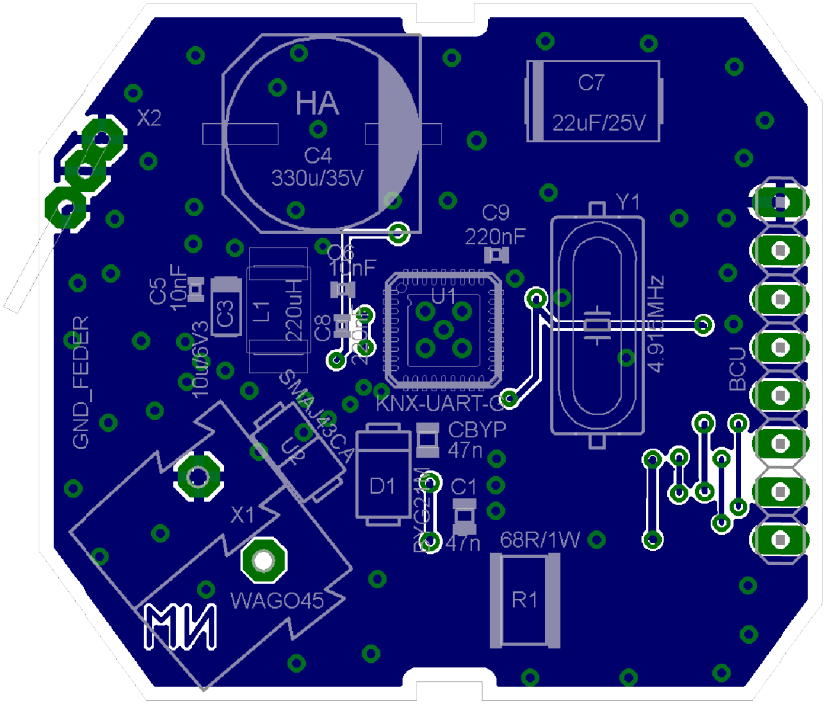

Figure 14 Layout Bottom View