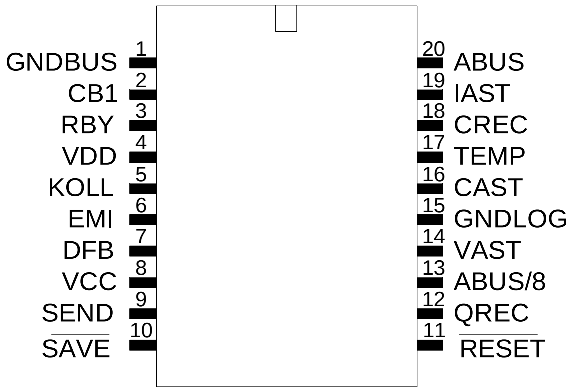
SIEMENS

TECHNICAL DATA

EIB-Twisted Pair Transceiver

FZE 1066 – EIB



Features

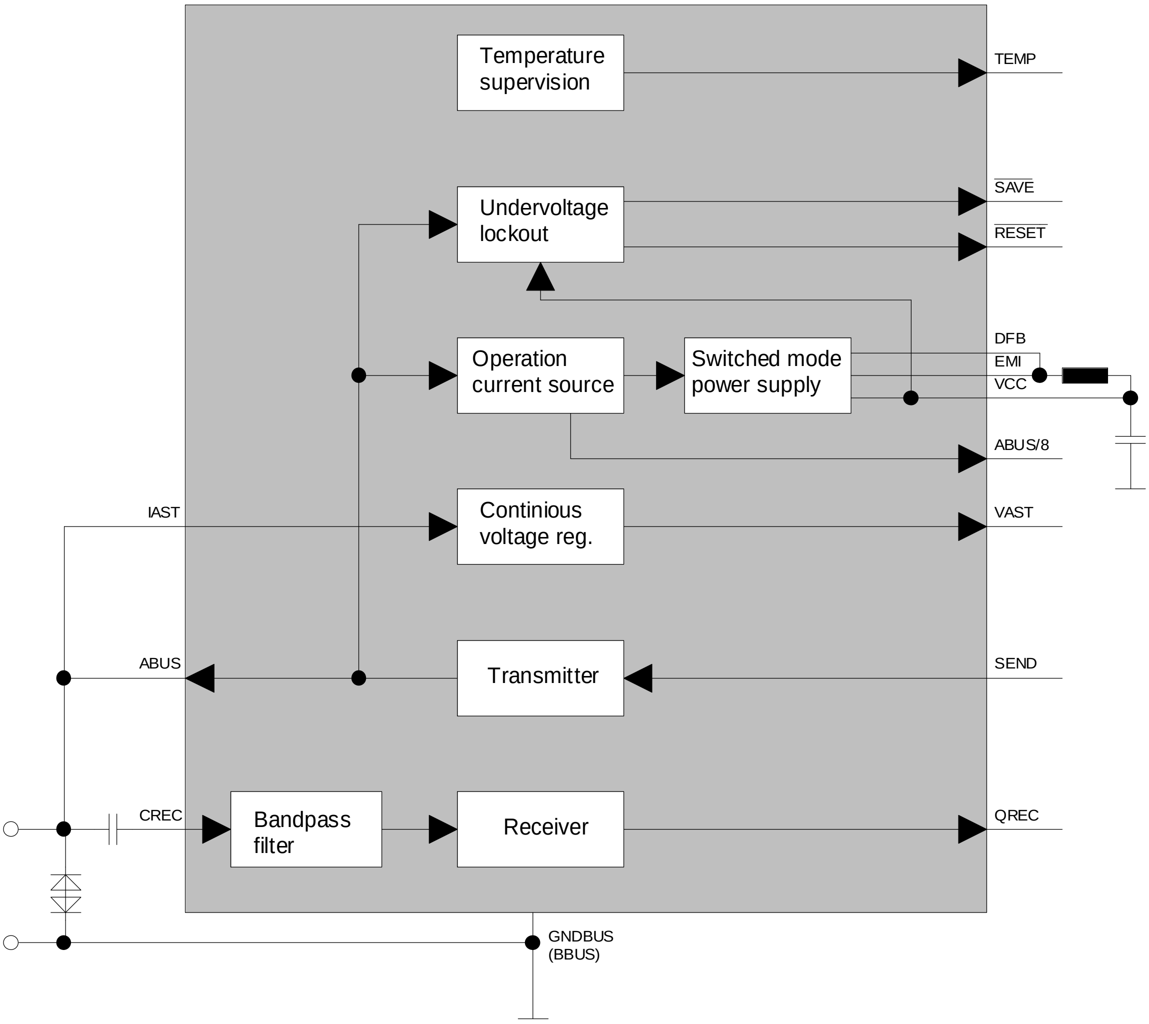
- EIB - Line driver
- EIB - Line receiver with hysteresis
- 5V switched-mode power supply
- Power-down reset (RESET)
- Under voltage lockout providing alarm signals (SAVE)
- 20 Pin SOP - package
- Operating temperature range - 25 to + 85 °C
- EIBA recognized component
- Temperature supervision
- According EIB specification
(EIBA Handbook Series, Release 3.0)
- Designed for use with MC68HC05B6 (EIB) and MC68HC705BE12 (EIB)

GENERAL DESCRIPTION

During transmitting the bus is loaded with current impulses which are converted to voltage impulses on the bus. The receiver converts the signals into digital signals. They are available on QREC.

*) The EIB is a two wire bus system designed for signal transmission as well as system power supply (DC).

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

SEND

The transmitter connects ABUS with VDD by a current source. As VDD is connected over a capacitor to GND, the current flows through the current source from ABUS to BBUS (GND).

The current source is superposed a limitation of the voltage pulse, because this current source is connected between ABUS and VDD. Therefore on a high resistant bus the voltage stroke is limited and on a low resistant bus the current stroke.

During a SEND operation the line behavior is monitored by the receiver.

On over temperature the transmitter is turned off by TEMP.

RECEIVE

The receiver consists of a differential comparator with hysteresis. It has an internal bandgap to suppress interference's from the Bus to the input comparator. On output QREC the regenerated digital signal is available.

TEMP

The temperature control protects the circuit during transmitting from being destroyed due to overheating. A short while before the circuit is getting over temperature, TEMP is switched from low to high. Thus the microprocessor gets enough time to finish the current transmission. As soon as the temperature decreases under an uncritical level the transmitter will be released.

If TEMP is low (logical) the real temperature in the circuit can be measured directly at the pin TEMP.

Typical points for temperature are :

Temperature	I_{TEMP}	TEMP Voltage in mV		
		Min	Typical	Max
- 25°C	1 µA	680	720	760
25°C	1 µA	600	640	680
75°C	1 µA	510	550	590
100°C	1 µA	460	500	540

VOLTAGE SUPPLY 20 V (VAST)

The voltage supply is current limited and short-circuit-proof. Therefore bus controlled components can be fed from this supply.

VOLTAGE SUPPLY 5 V (VCC)

The voltage supply is also current limited and short-circuit-proof. The voltage is generated with a switched mode power supply in order to get a high efficiency. With this voltage supply the circuit itself and additional components can be supplied.

OPERATION CURRENT SOURCE (BSQ)

The BSQ has the following tasks :

+ Regulation of pre-stabilized voltage V_{VDD} to V_{ABUS} – 8 V
+ Generation of compensation impulse on bus, generated by dropping the actually current demand of component
+ Protect capacitor between VDD and GND, which is loaded on transmitting, from overloading

SEQUENTIAL CONTROL

The sequential control is responsible for the softstart. It generates an internal supply as long as the integrated circuit dos not get voltage from V_{VCC}. The sequential control measures the voltage on V_{VDD} and V_{VCC}, by a comparator with hysteresis the signals RESET and SAVE are generated.

RESET is logical low if V_{VCC} is too low

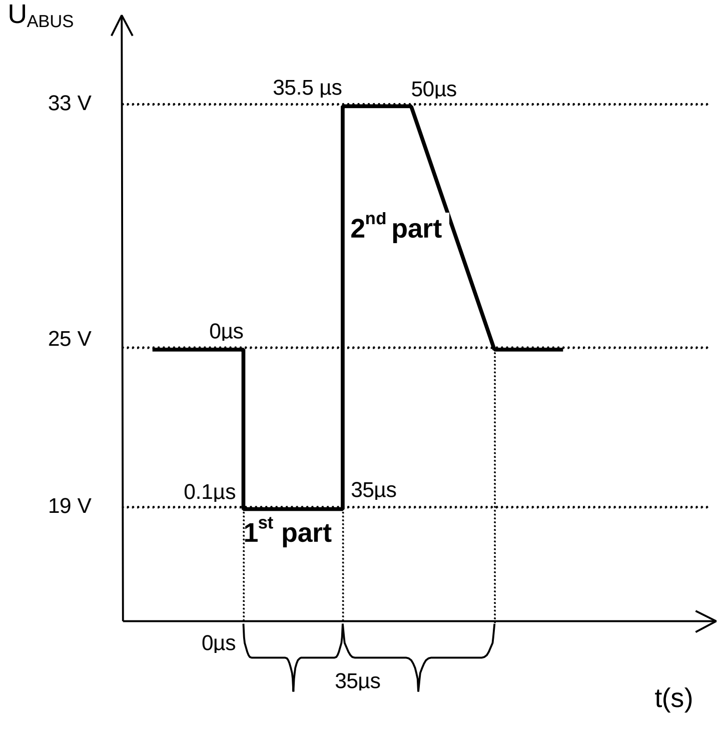
SAVE is logical low if V_{VCC} or V_{VDD} is too low

UNDERVOLTAGE LOCKOUT

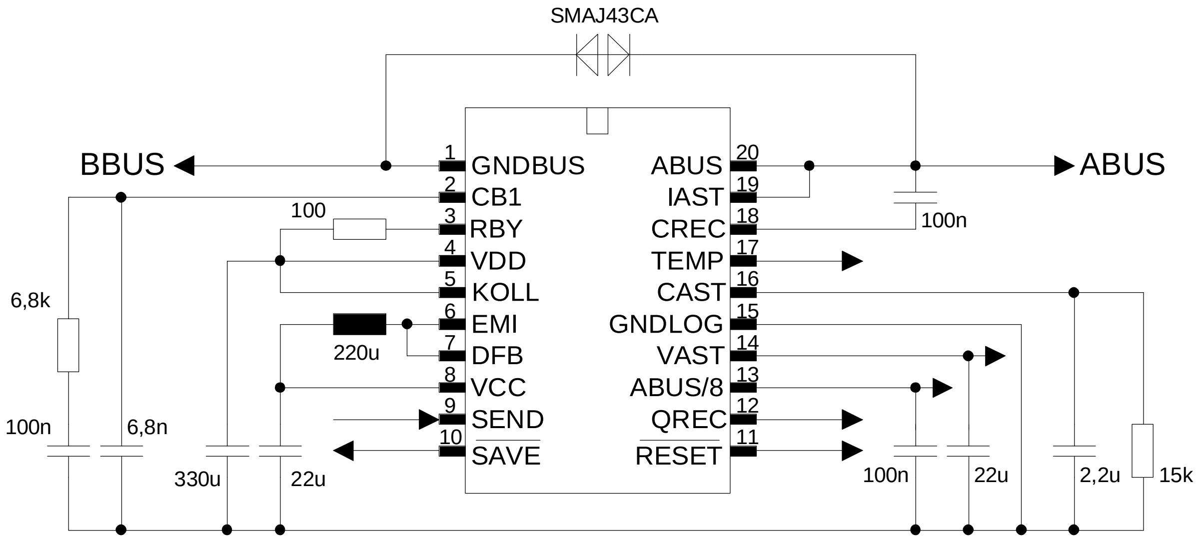
SAVE provides a power-down pre-alarm. As soon as the voltage of the buffer capacitor drops below the threshold (approx.18 V), SAVE goes low.

RESET and SAVE will go low, if the 5 V supply VCC is to low.

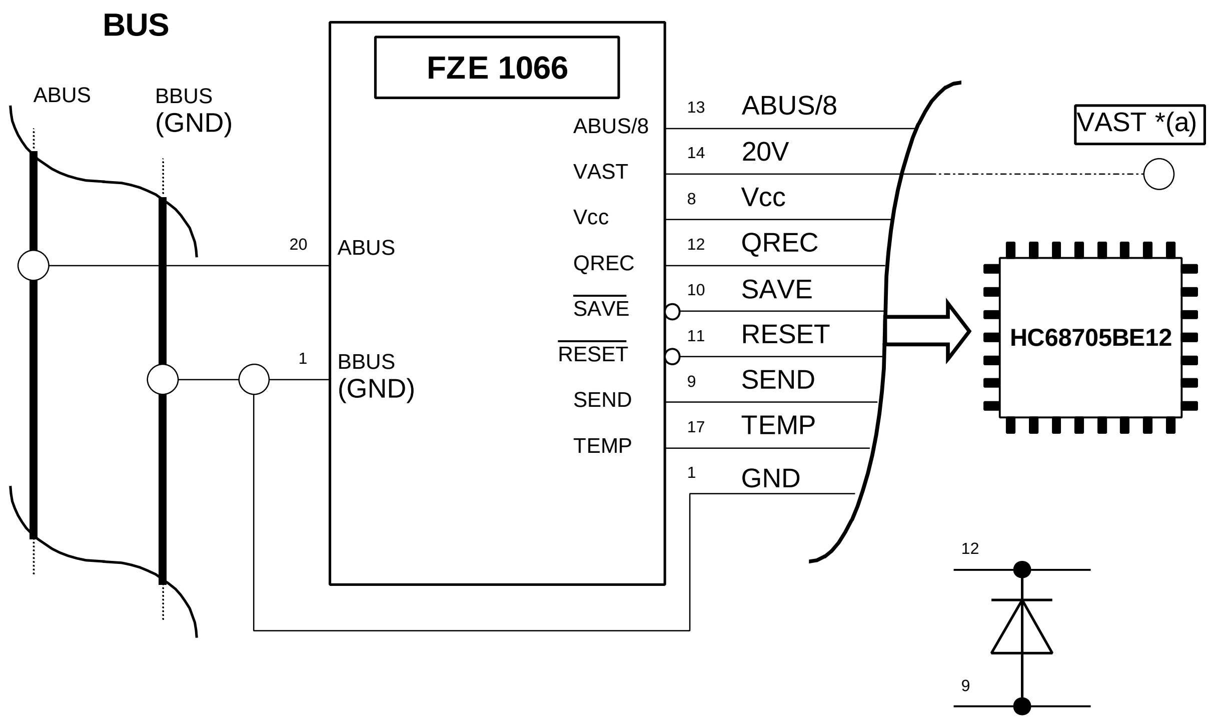
Bus Norm Impulse



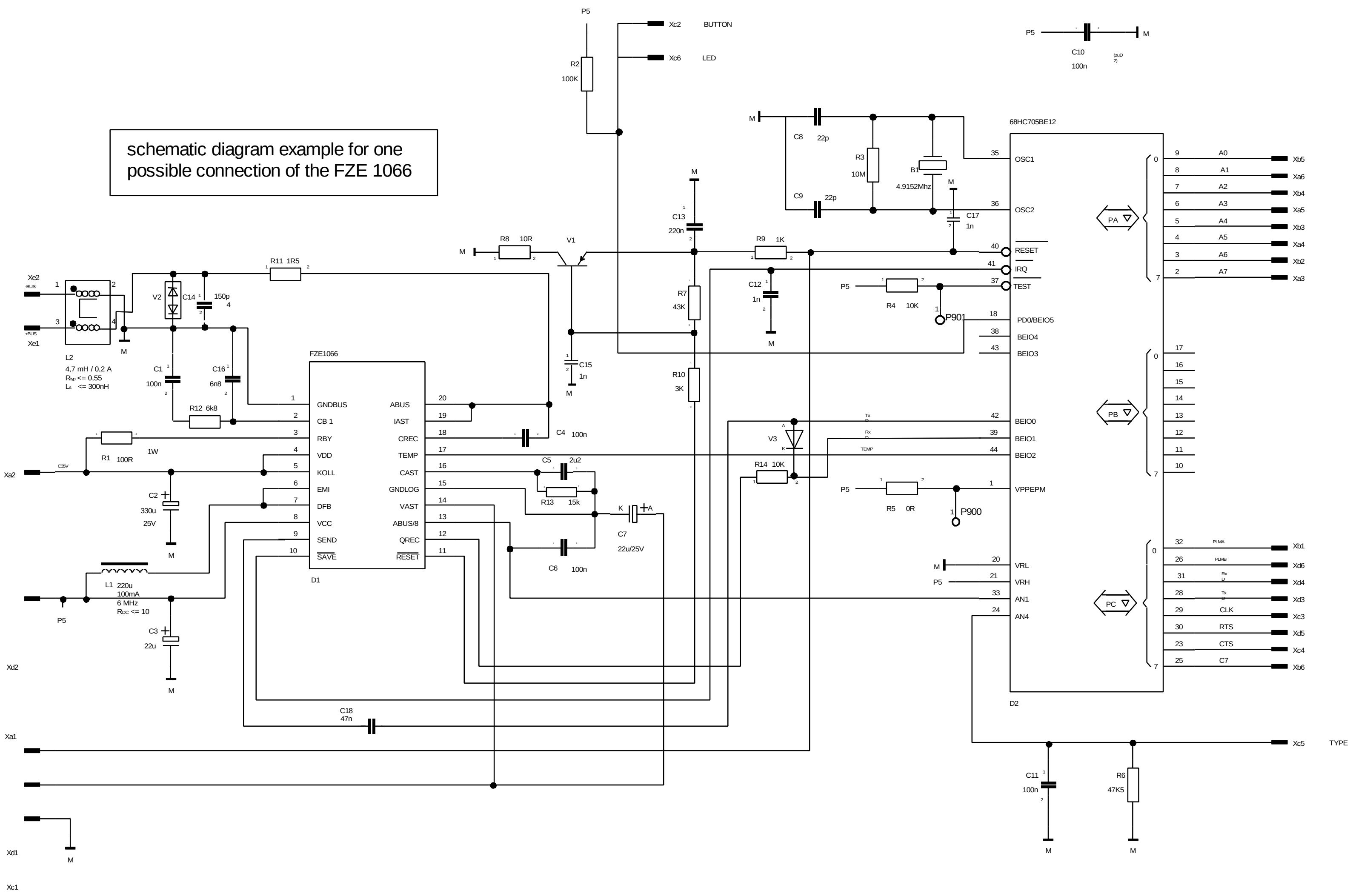
TYPICAL APPLICATION CIRCUIT



INTERFACE DESCRIPTION



**(a) If an application is connected, Pin 14 (V_{VAST}) serves for voltage supply of this application*

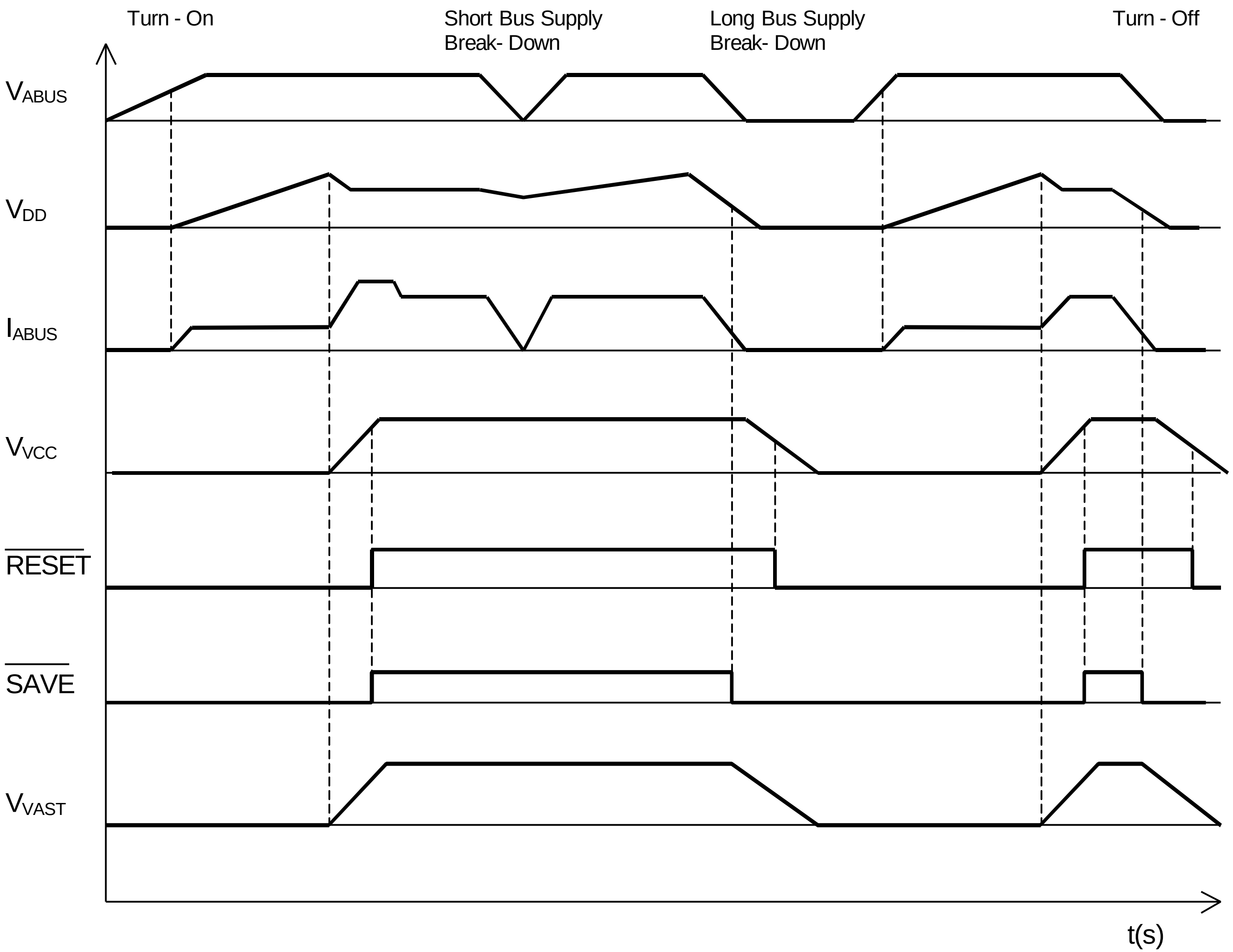

schematic diagram example for one possible connection of the FZE 1066
FZE1066
D1
68HC705BE12
D2
GNDBUS
CB 1
RBY
VDD
KOLL
EMI
DFB
VCC
SEND
SAVE
ABUS
IAST
CREC
TEMP
CAST
GNDLOG
VAST
ABUS/8
QREC
RESET
OSC1
OSC2
RESET
IRQ
TEST
PD0/BEIO5
BEIO4
BEIO3
BEIO0
BEIO1
BEIO2
VPPEPM
VRL
VRH
AN1
AN4
PA
PB
PC
A0
A1
A2
A3
A4
A5
A6
A7
CLK
RTS
CTS
C7
BUTTON
LED
TYPE
L2
4,7 mH / 0,2 A
L1 220u
100mA
6 MHz
B1
4.9152Mhz
C7
22u/25V
P900
P901

PARTLIST *)

No.	Component	Type/Value	Remarks
R1	Resistor	100R/5%	1000mW
R2	Resistor	100K/5%	50mW
R3	Resistor	1M/5%	50mW
R4	Resistor	10K/5%	50mW
R6	Resistor	47K5/1%	50mW
R7	Resistor	43K/5%	50mW
R8	Resistor	10R/5%	50mW
R9	Resistor	1K/5%	50mW
R10	Resistor	3K/5%	50mW
R11	Resistor	1R5/5%	250mW
R12	Resistor	6K8/5%	50mW
R13	Resistor	15K/5%	50mW
R14	Resistor	10K/5%	50mW
C1, C4, C6, C10, C11	Capacitor	100n/5%/50V	Ceramic
C2	Capacitor	330u/20%/25V	Electrolytic,
C3	Capacitor	22u/20%/6V ESR < 0,7 (100kHz) $I_{riplmax}$ > 100 mA	Electrolytic,
C5	Capacitor	2u2/10%/6V	Electrolytic,
C7	Capacitor	22u/20%/25V	Electrolytic,
C8, C9	Capacitor	22p/5%/50V	Ceramic
C12, C15, C17	Capacitor	1n/10%/50V	Ceramic
C13	Capacitor	220n/10%/25V	Ceramic
C14	Capacitor	150p/5%/50V	Ceramic
C18	Capacitor	47n//10%/50V	Ceramic
L1	Choke	220u/100mA/6MHz $R_{DC} \leq 10\ \Omega$	
L2	Choke	4,7mH/0,2A $R_{typ} \leq 0{,}55\ \Omega$, $L_S \leq 300$ nH	
V1	Transistor	BC807-40	
V2	Suppressor-Diode	SMAJ43CA	
V3	Diode	LL4148	
B1	Quarz	4.9152MHz/50ppm/30pF	
D2	Microcontroller	MC68HC705BE12	Motorola
D1	IC	FZE 1066	Siemens (Infineon)

*) additional components may be required because of EMV

DIAGRAM with RESET and SAVE



PIN DESCRIPTION

PIN	FUNCTION	SYMBOL	Units	Min	Max	Remarks
1	Ground high current, EIBus negative voltage input	GNDBUS				
2	VDD control loop capacitor	CB1				
3	Bypass 70 mA VDD to GND	RBY				
4	$V_{VDD} = V_{ABUS}$ – 8V stabilized	VDD	V	V_{ABUS} -9	V_{ABUS} -7	3 mA ≤ I_{ABUS} ≤ 25 mA
5	Collector SMPS – transistor	KOLL				
6	Emitter SMPS – transistor	EMI				
7	Clamping diode for SMPS	DFB				
8	VCC (5V) control loop input	VCC	V	4.7	5.3	0 mA ≤ I_{VCC} ≤ 30 mA
9	Transmitter input	SEND	V	Vcc-0.3 -V_{BE}	VCC 0.3	High, I_{SEND} ≤ 150 µA Low, I_{SEND} < 100 µA
10	Low on V_{VDD} < 9.5 V, or V_{VCC} < 4.5 V	SAVE	V	Vcc-0.5 -V_{BE}	VCC 0.5	High, I_{SAVE} = -1 mA Low, I_{SAVE} = 1 mA
11	Low on Vcc < 4.5 V	RESET				
12	Receiver output	QREC	V	 V_{VCC}-1	0.5	Low voltage output, I_{QREC} = 1mA High voltage output, I_{QREC} = 1mA
13	V_{ABUS} divided by 8	VABUS	V	3	3.25	V_{ABUS} =25V, I_{ABUS} = 1nA
14	20 V output	VAST	V	18	22	21V < V_{ABUS} < 30V, 0mA < -I_{VAST} < 5mA
15	GROUND low current	GNDLOG				
16	VAST control loop capacitor	CAST				
17	Temperature supervision output	TEMP	V	0.6 V_{VCC}-0.5	0.68 V_{VCC}	Low (25°C), I_{TEMP} = 1 µA High (130°C), 0,3 mA ≤ I_{TEMP} ≤ 3 mA
18	RECEIVER input	CREC	V	-0.45 -0.1	-0.7 -0.35	QREC goes high QREC goes low
19	20V input	IAST	V			$V_{IAST} = V_{ABUS}$
20	EIBus positive voltage input	ABUS	V	20	33	

ABSOLUTE MAXIMUM RATINGS

The maximal ratings may not be exceed under circumstances, not even momentarily and individually, as permanent damage to the IC will result.

All voltages referred to GND

Pin		Symbol	Min	Max	Unit
1	GND				V
2	CB 1 voltage	$V_{CB\ 1}$	-0.3	6	V
3	RBY voltage	V_{RBY}	-0.3	33	V
4	VDD voltage	V_{VDD}	-0.3	33	V
5	KOLL voltage	V_{KOLL}	-0.3	33	V
6	EMI voltage	V_{EMI}	-0.3	33	V
7	DFB voltage	V_{DFB}	-0.3	33	V
8	VCC voltage	V_{VCC}	-0.3	6	V
9	SEND voltage	V_{SEND}	-0.3	V_{ZSEND}	V
10	SAVE voltage	V_{SAVE}	-0.3	6	V
11	RESET voltage	V_{RESET}	-0.3	6	V
12	QREC voltage	V_{QREC}	-0.3	6	V
13	ABUS/8 voltage	$V_{ABUS/8}$	-0.3	6	V
14	VAST voltage	V_{VAST}	-0.3	25	V
15	GND	GND			
16	CAST voltage	V_{CAST}	-0.3	6	V
17	TEMP voltage	V_{TEMP}	-0.3	6	V
18	CREC voltage	V_{CREC}	-0.3	45	V
19	IAST voltage	V_{IAST}	-45	45	V
20	ABUS voltage	V_{ABUS}	-45	45	V

ELECTRICAL SPECIFICATION

Storage Temperature - 60 ... 125 °C

Operating Temperature - 25 ... 85 °C

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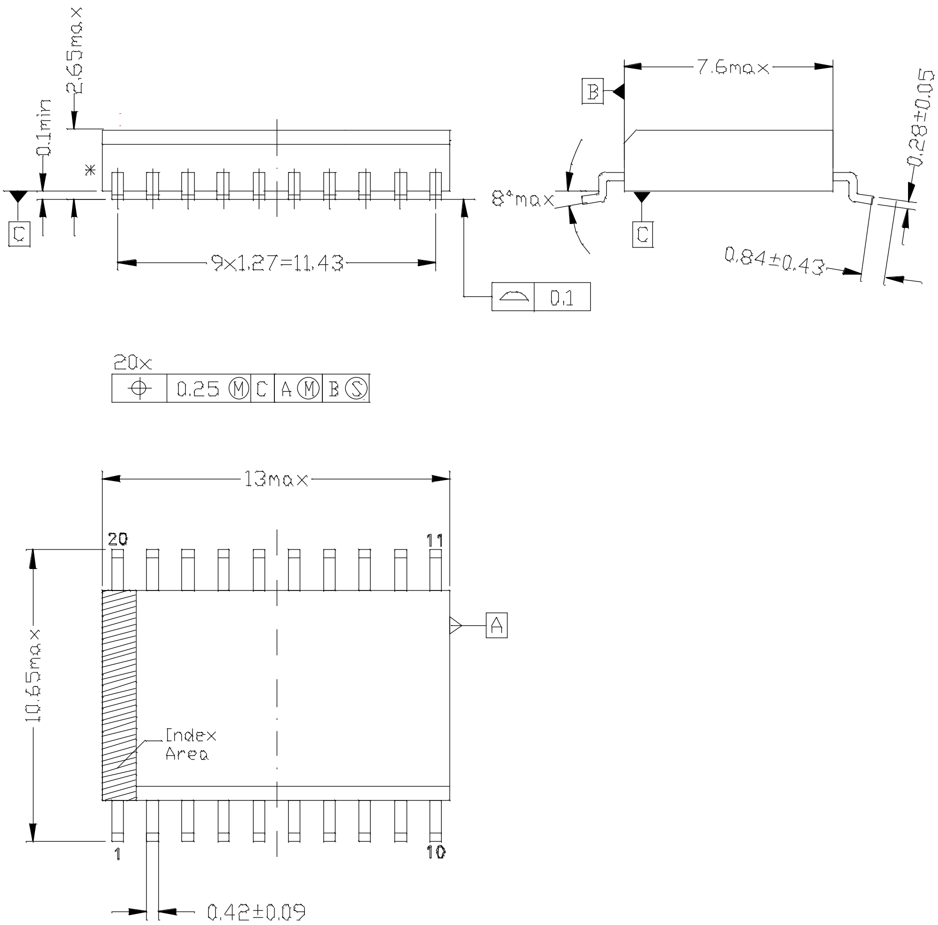
MECHANICAL SPECIFICATION



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